

PG150-C03

384b GDDR6 x16

TALL DP + DP + DP + HDMI/DP + USB

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A

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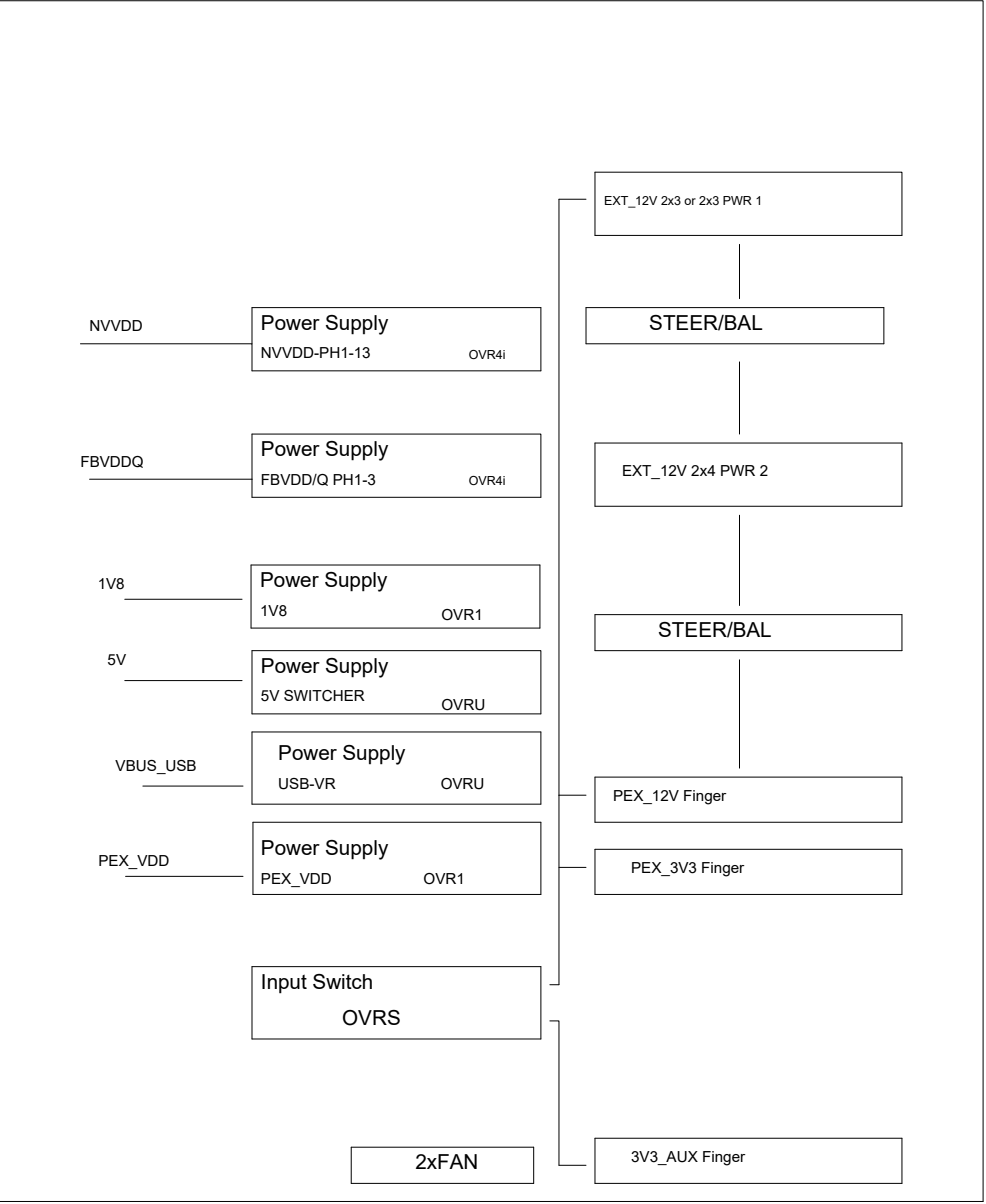
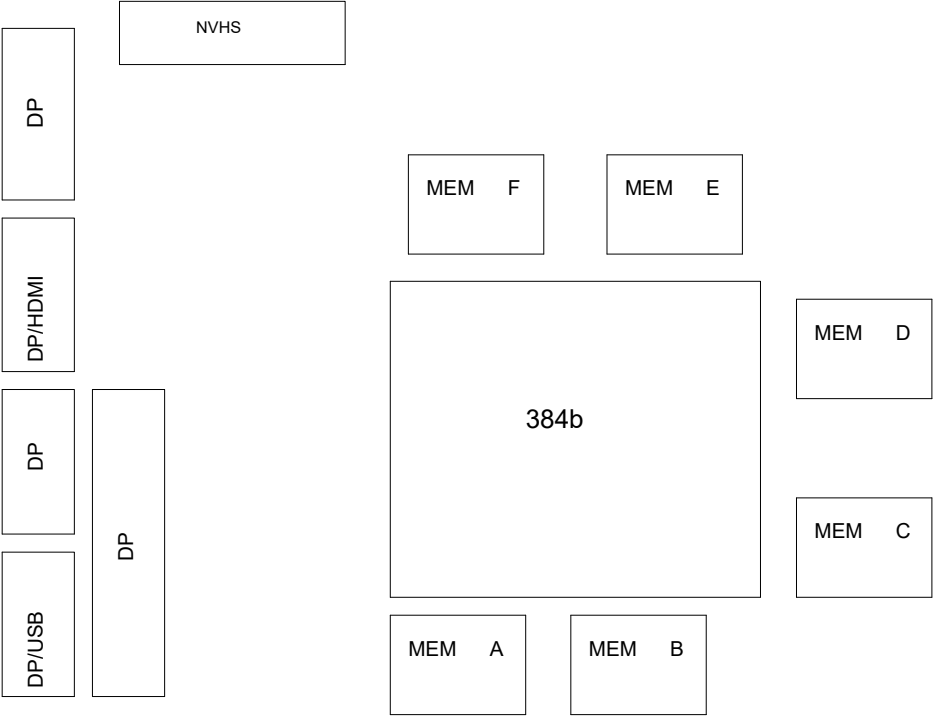
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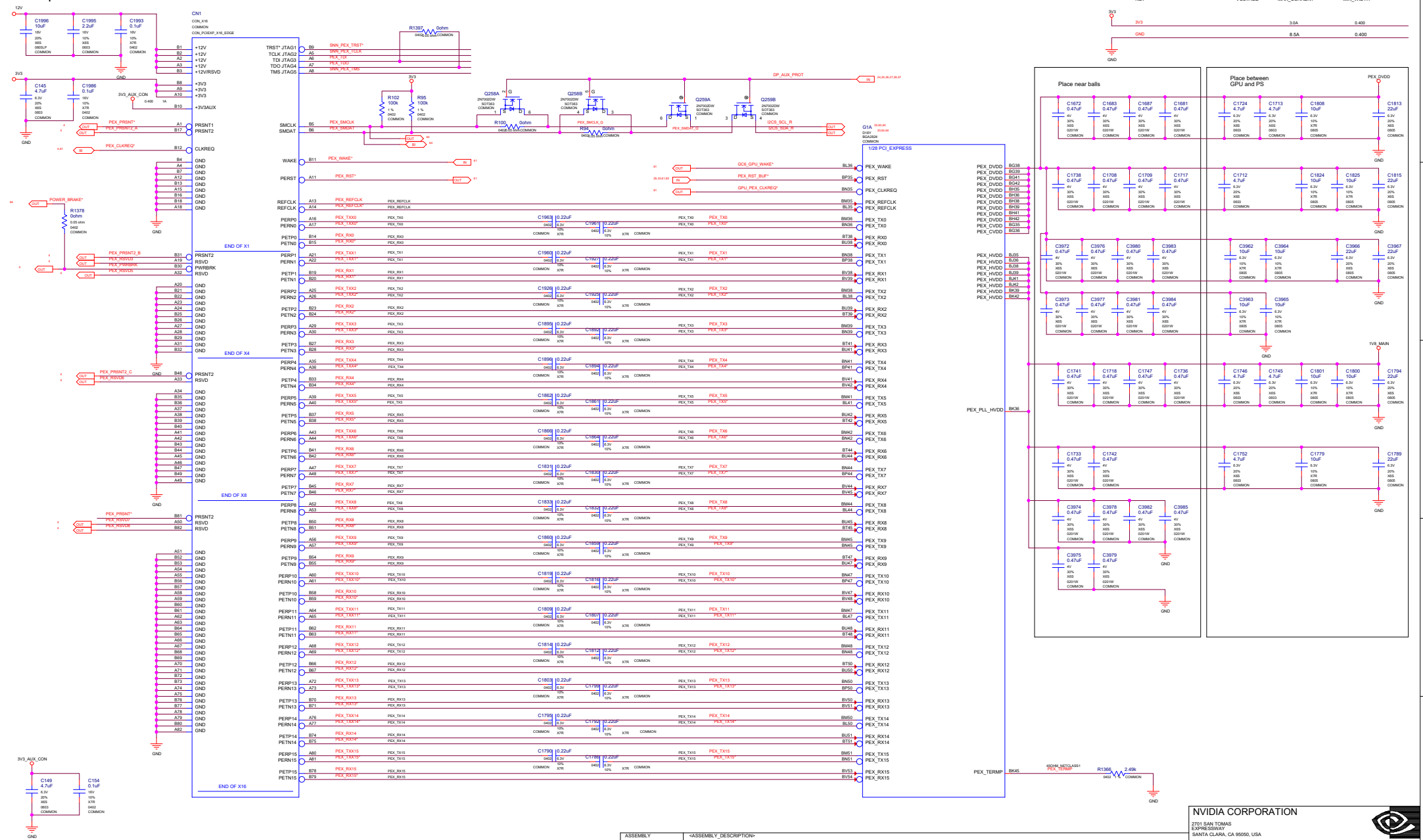
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PCI Express



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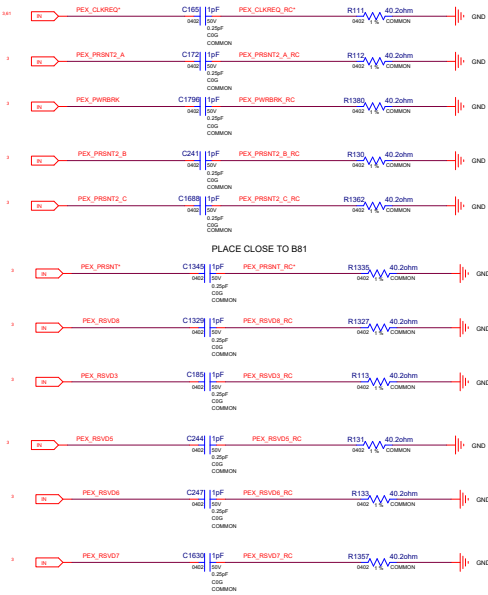


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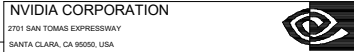
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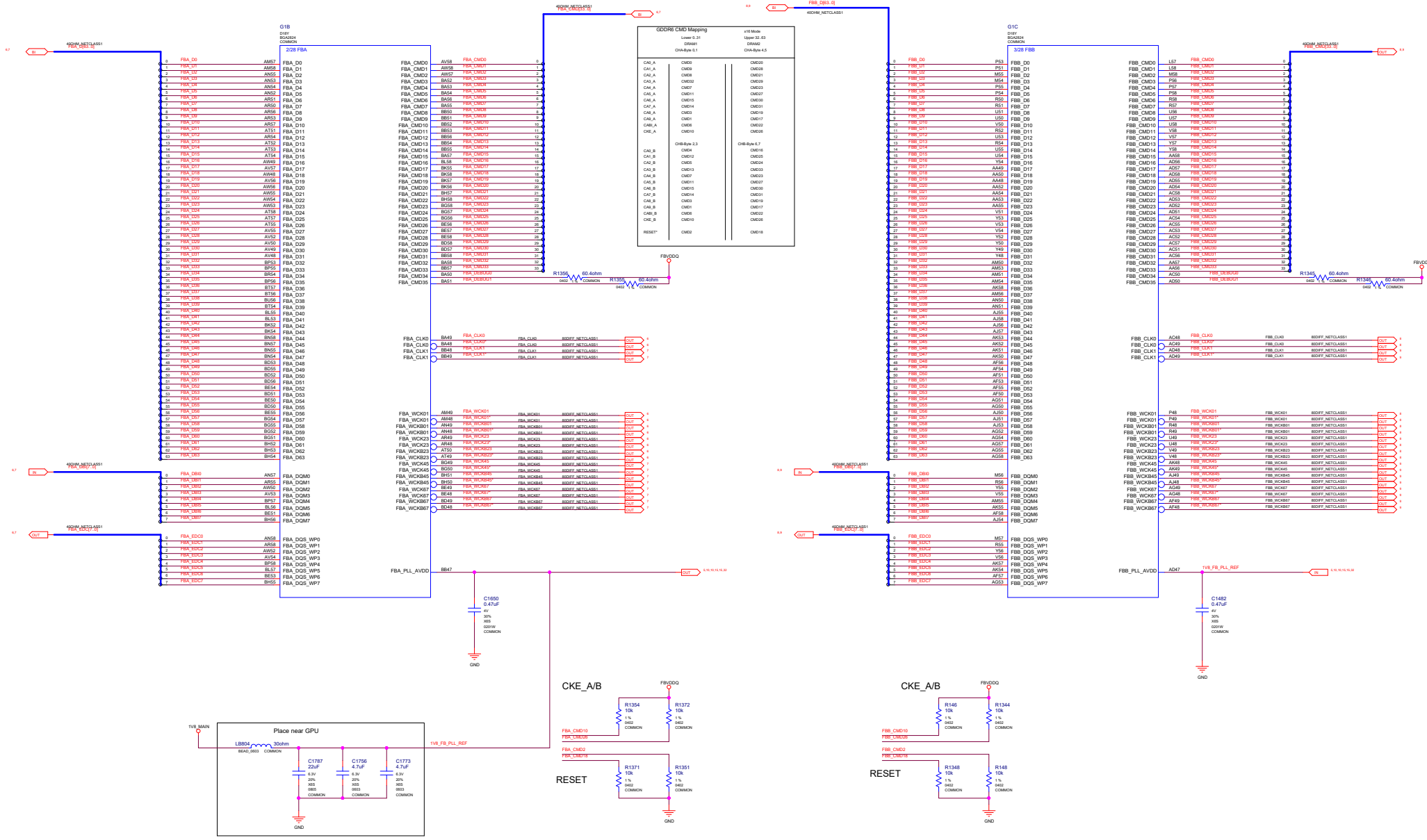


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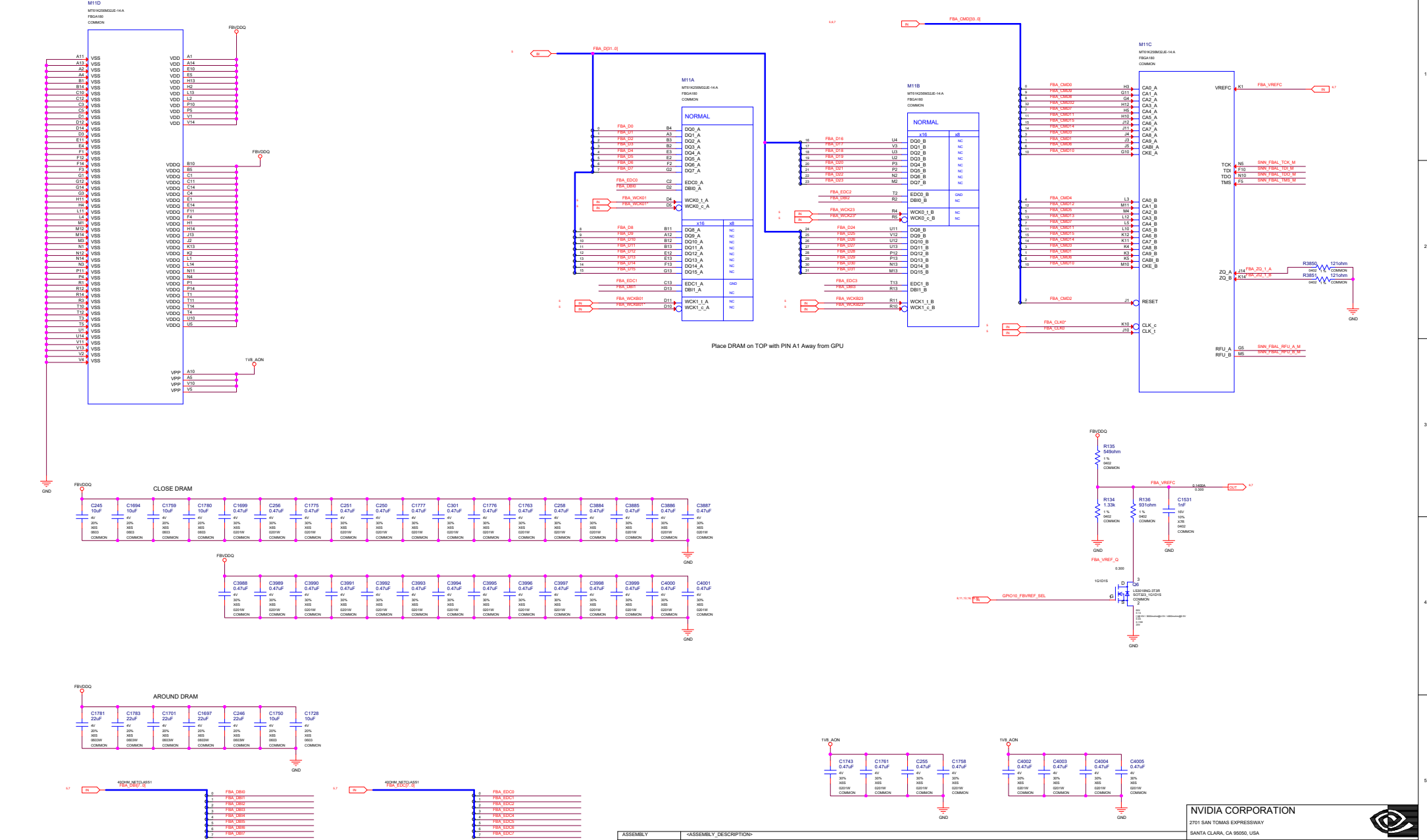
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MEMORY: GPU Partition A/B



ASSEMBLY	<ASSEMBLY_DESCRIPTION>
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MEMORY: FBA Partition 31..0



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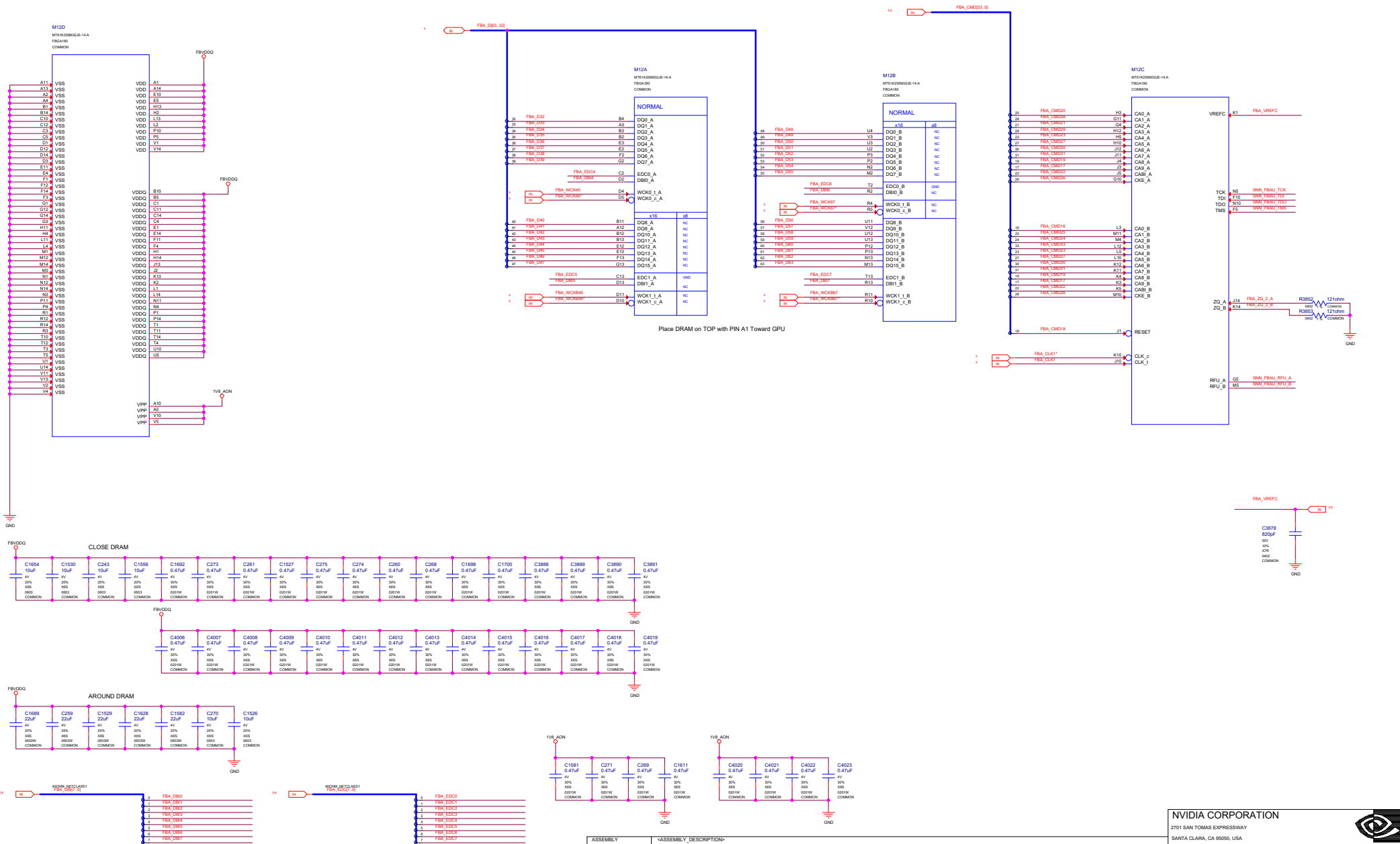
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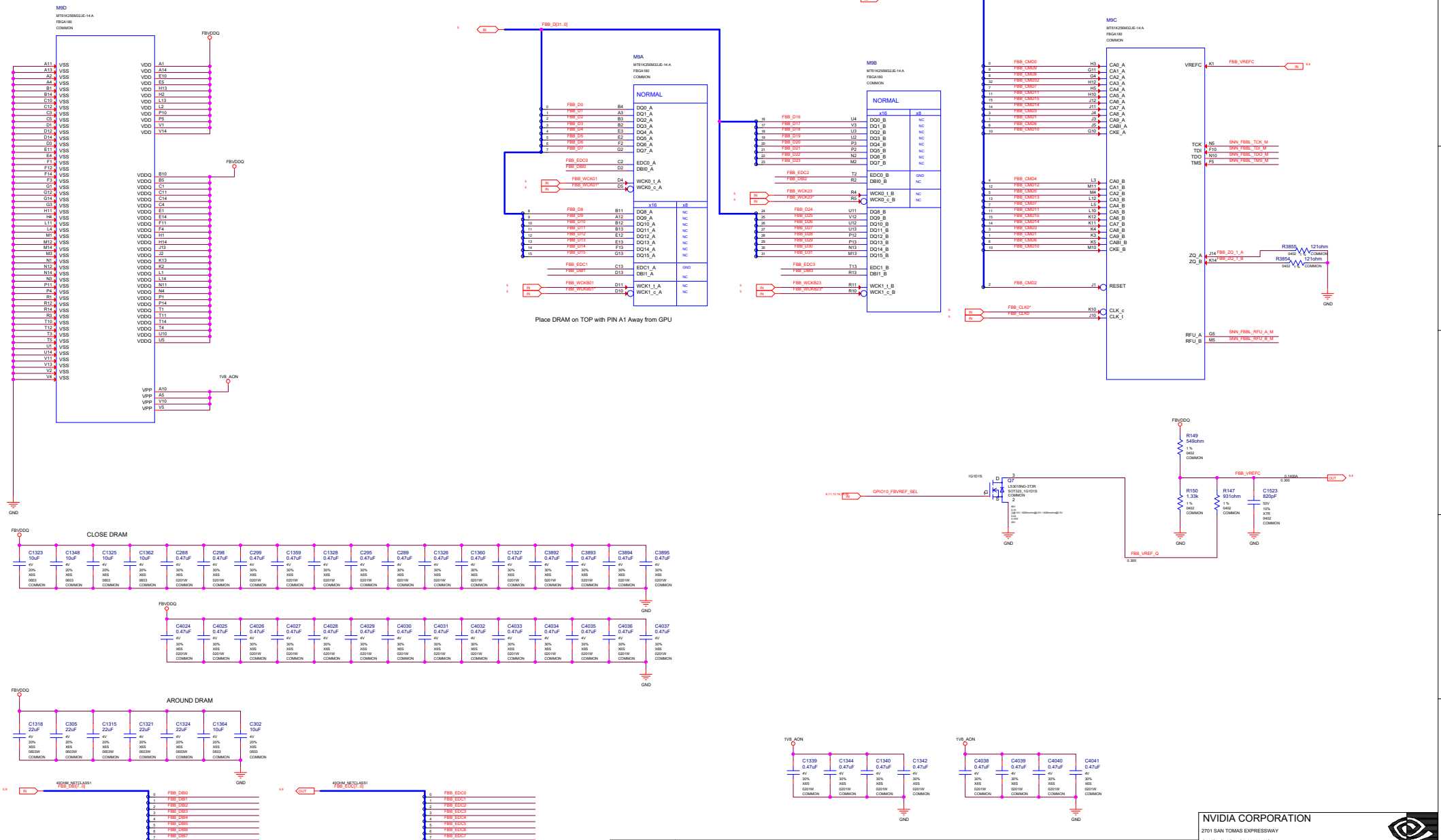


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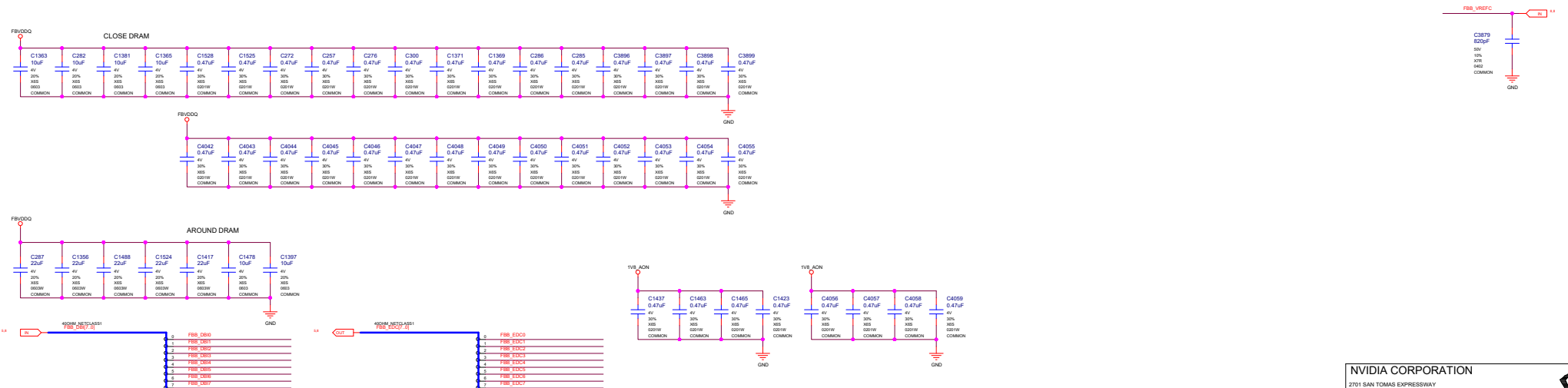
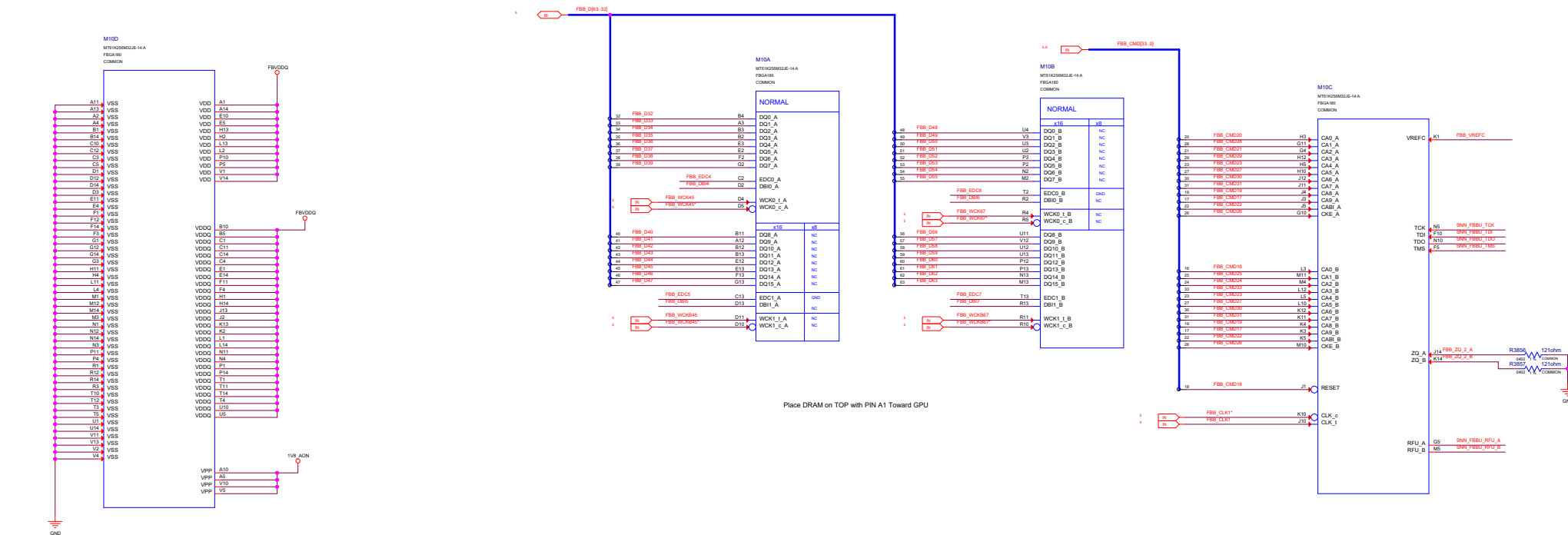
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MEMORY: FBB Partition 31..0




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MEMORY: FBB Partition 63..32

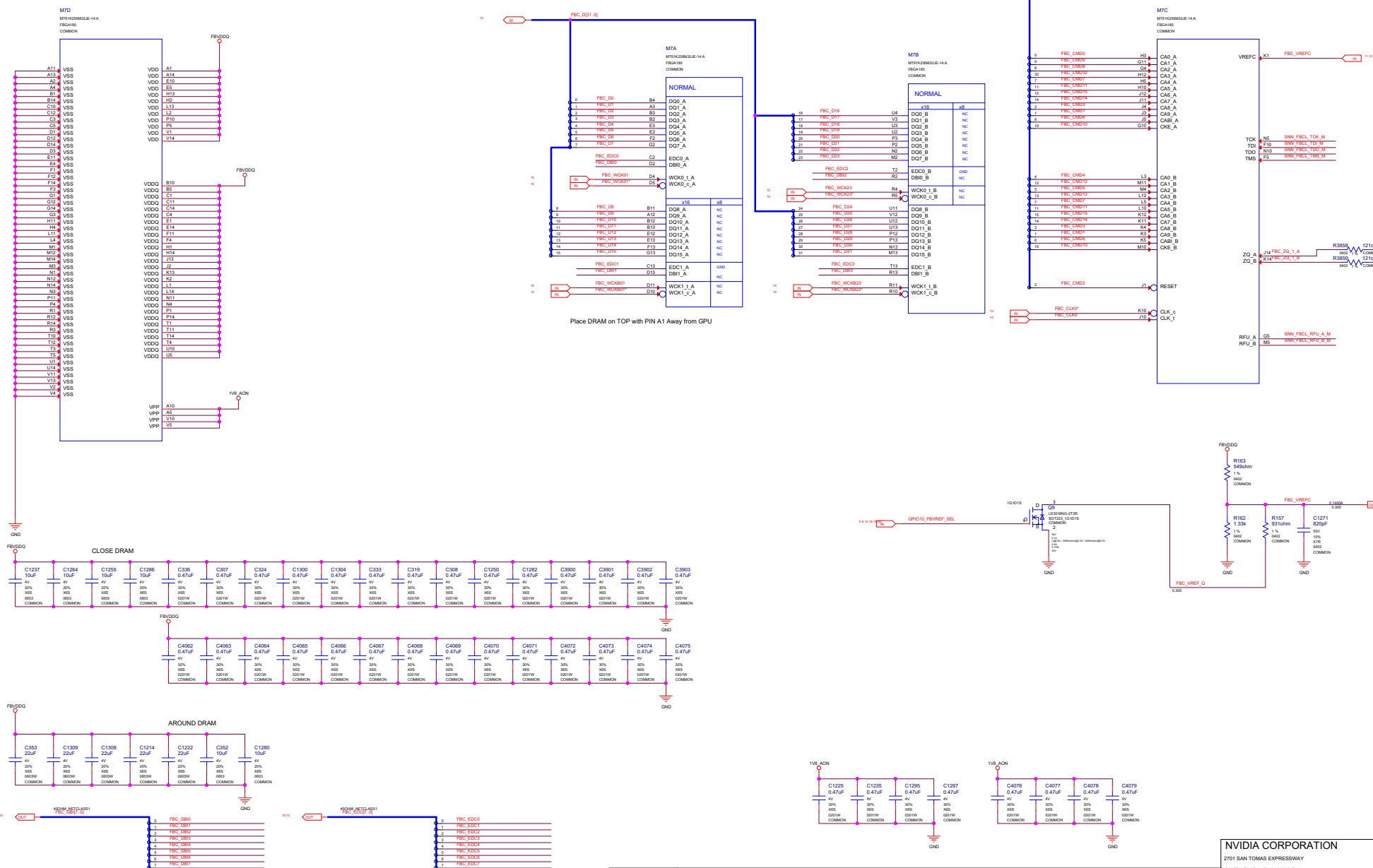


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MEMORY: FBC Partition 31..0



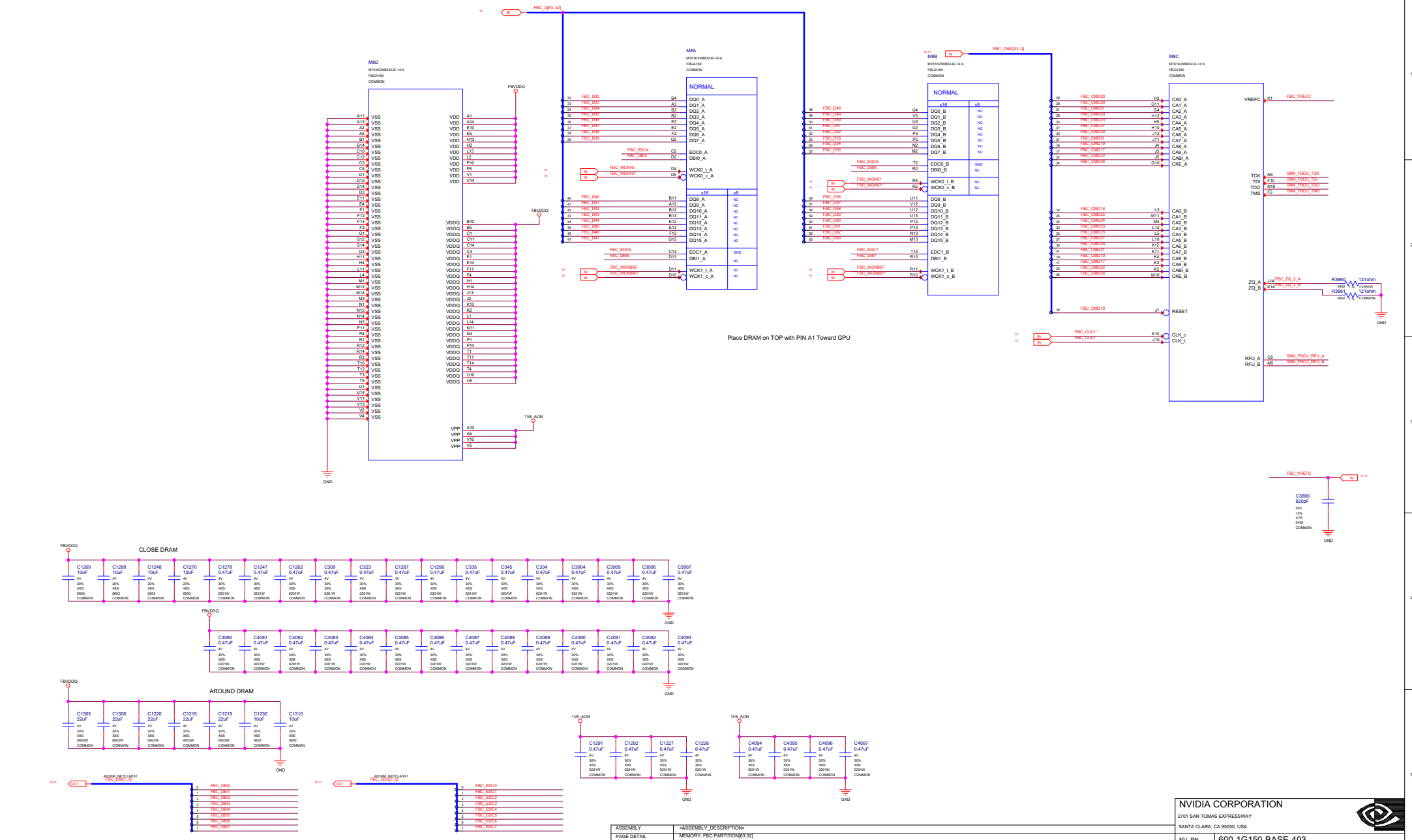
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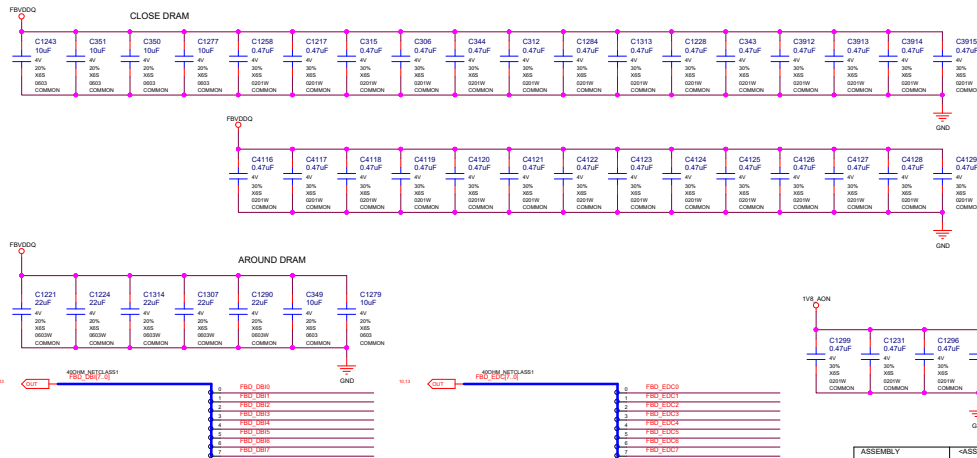
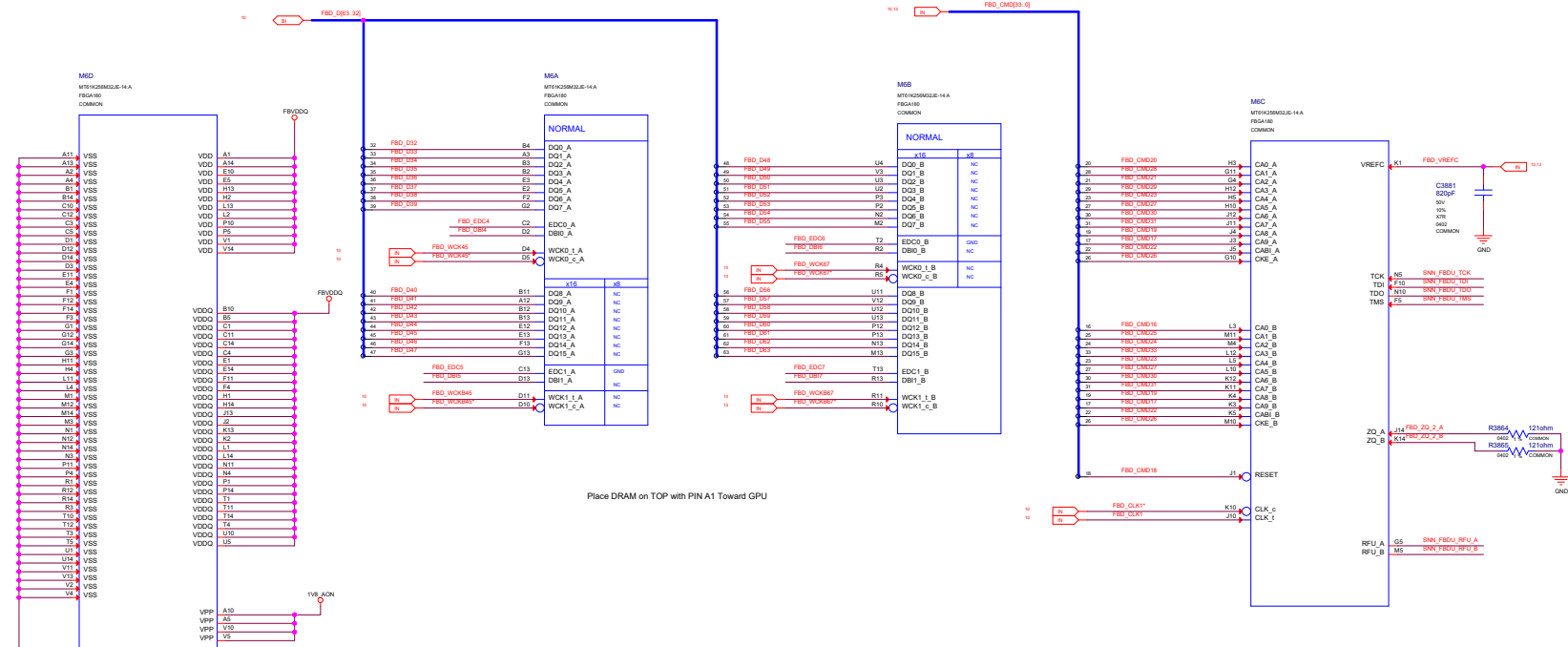
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MEMORY: FBC Partition 63..32




MEMORY: FBD Partition 63..32



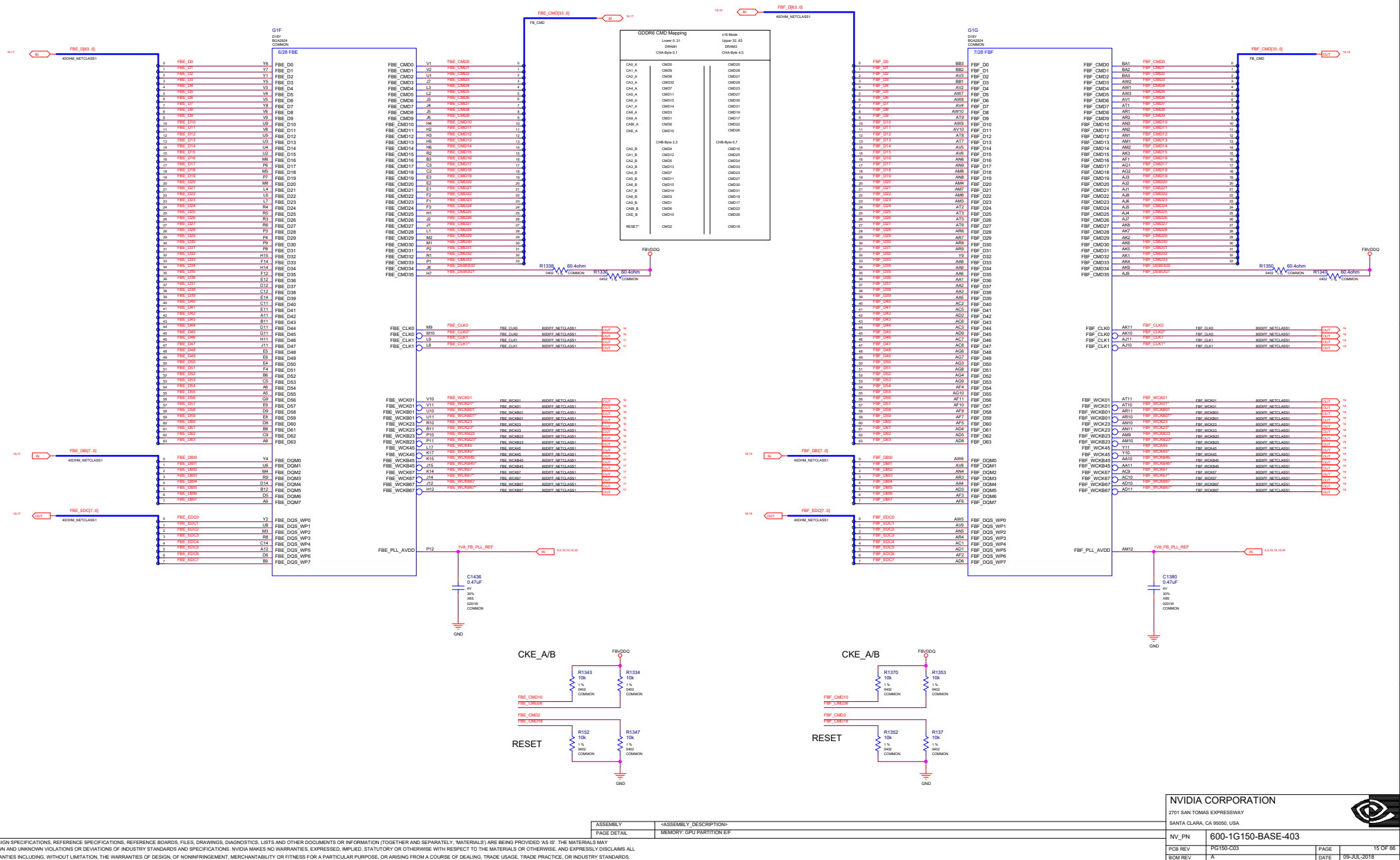
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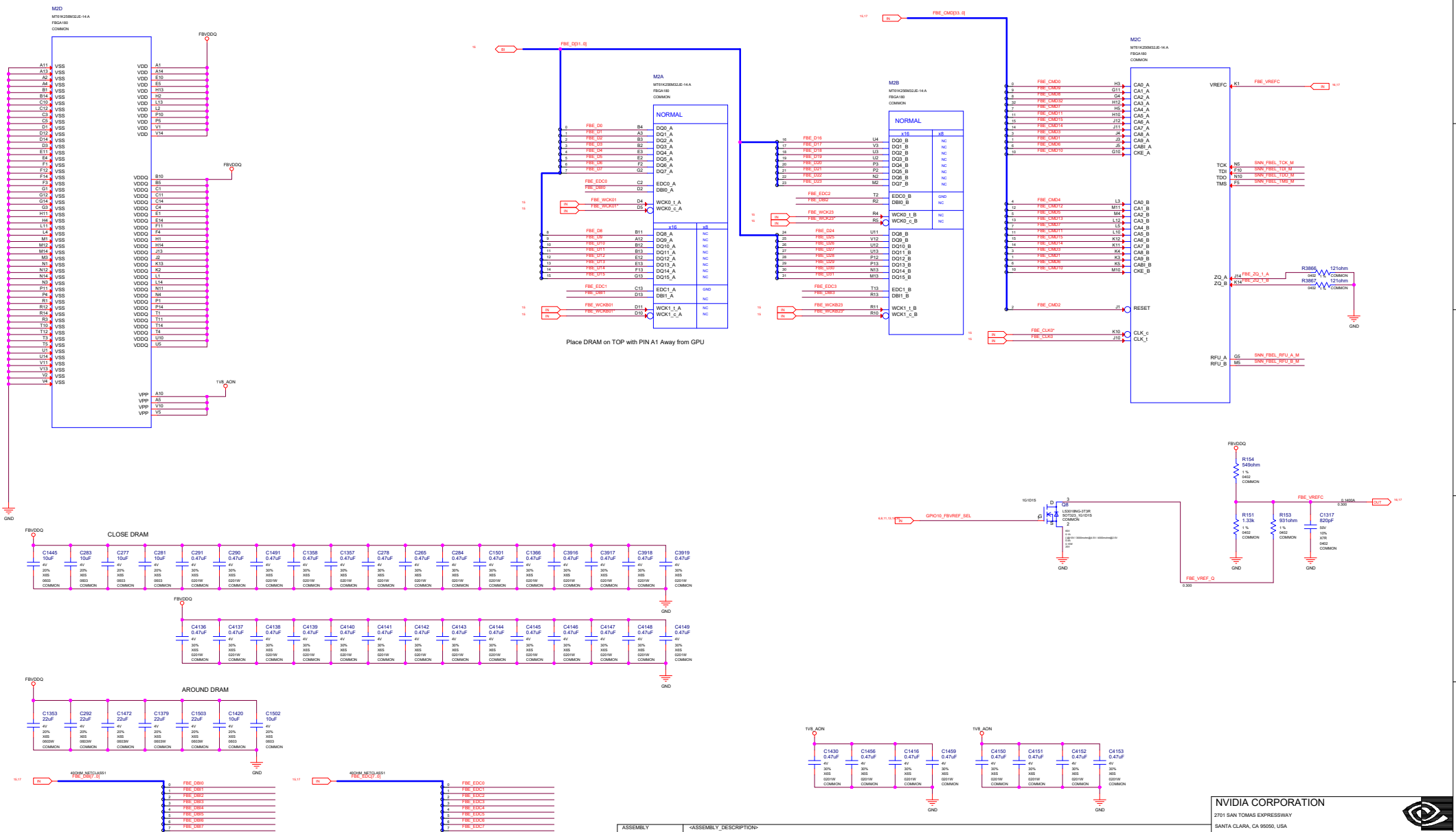


MEMORY: GPU Partition E/F




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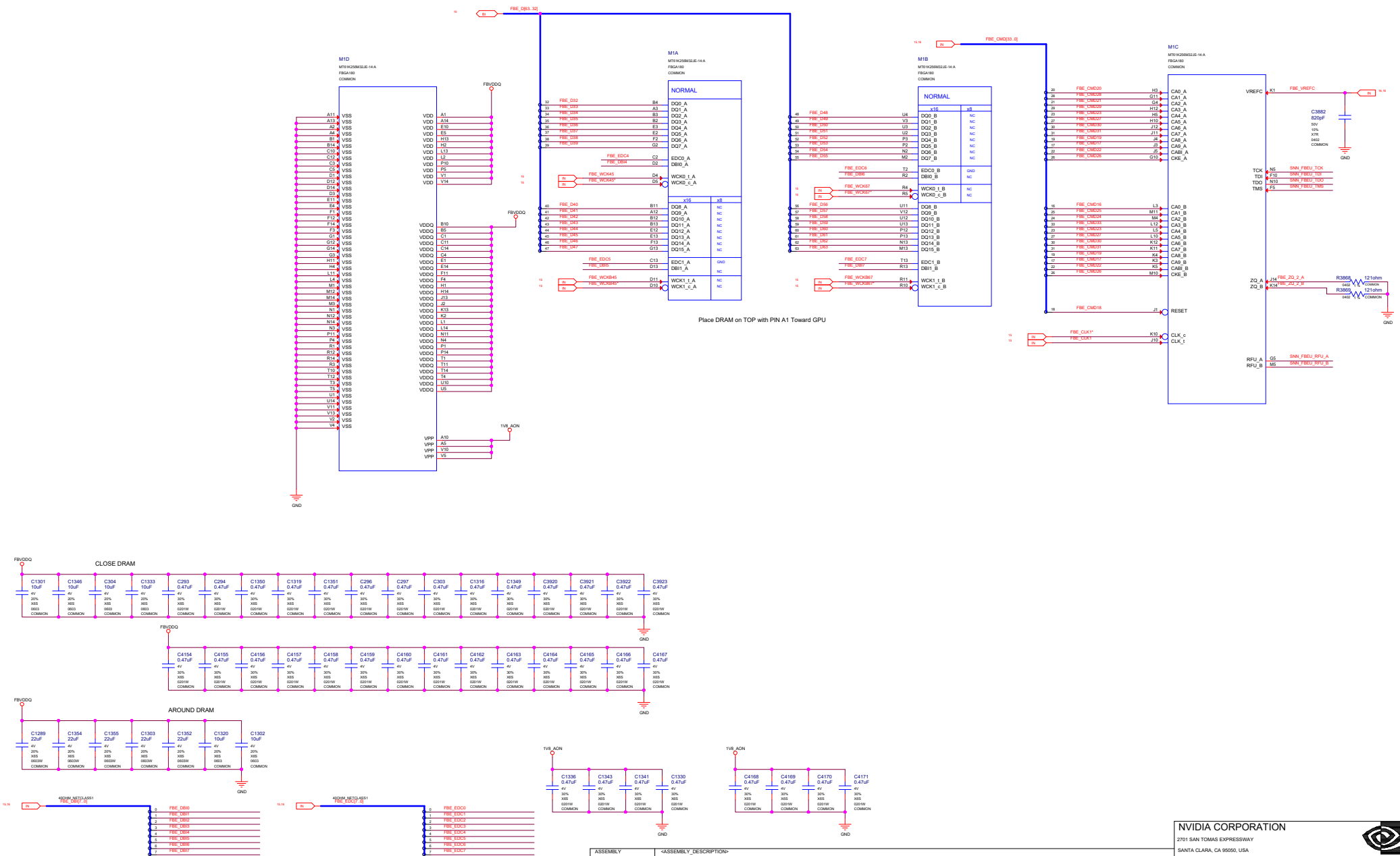


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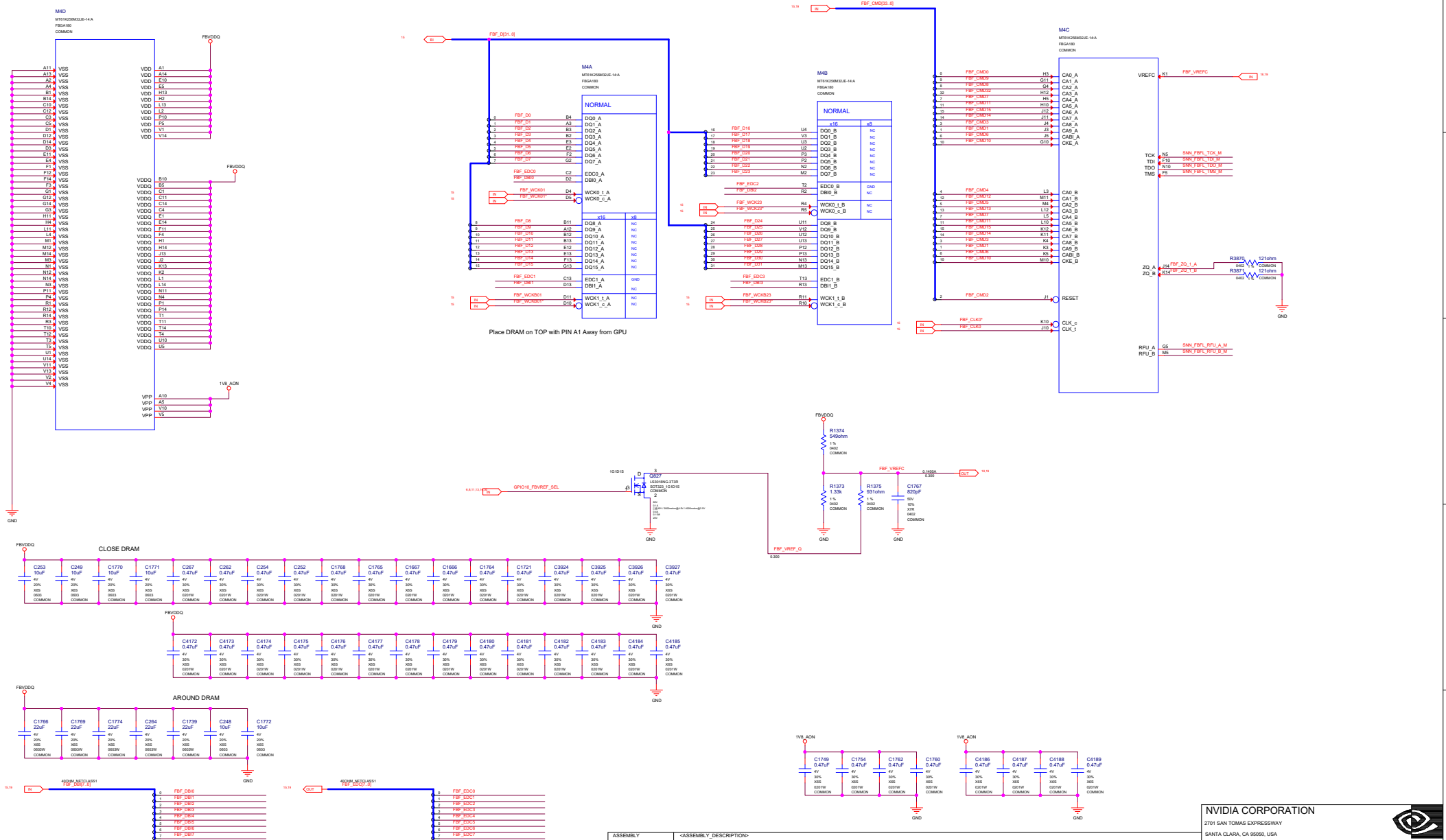
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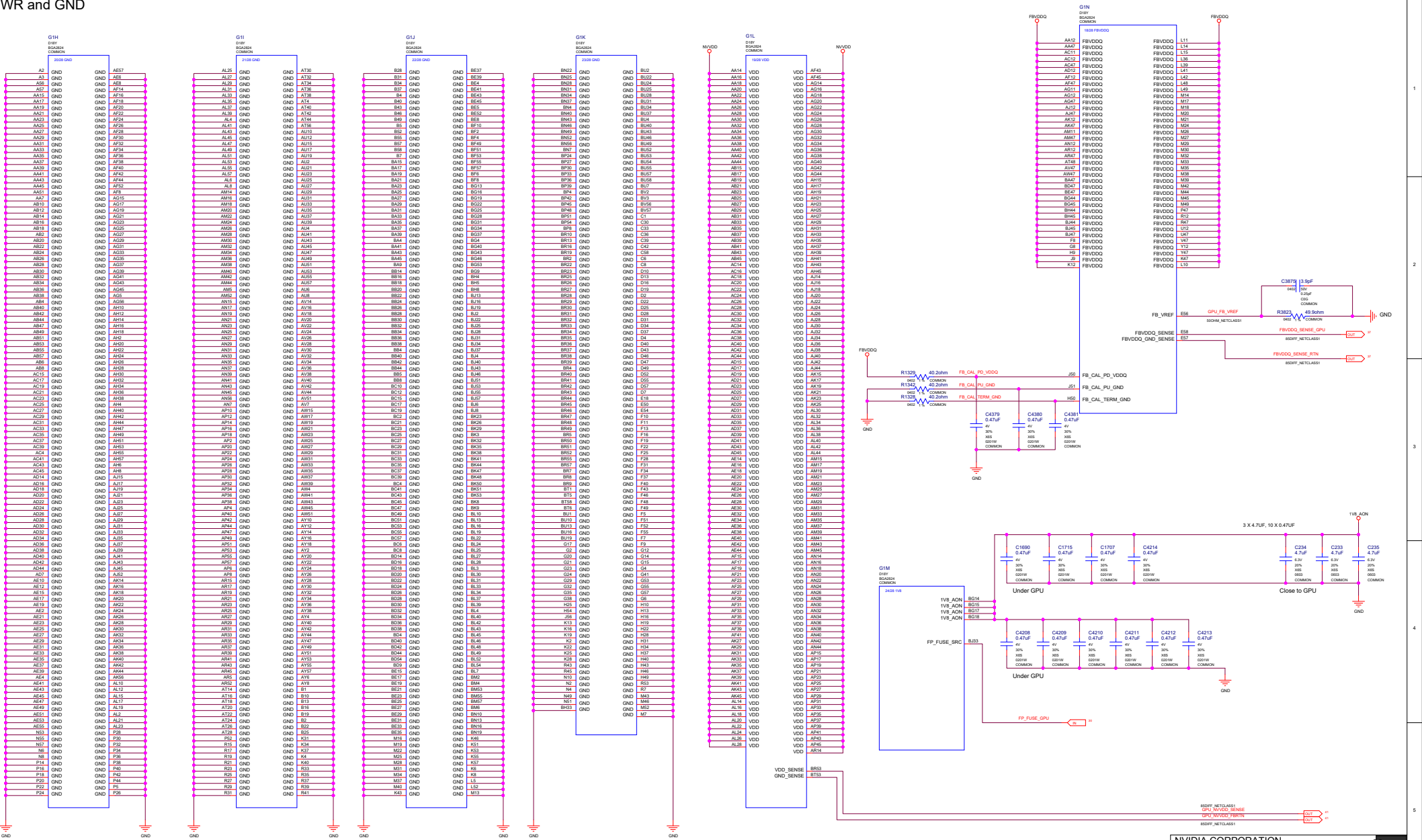


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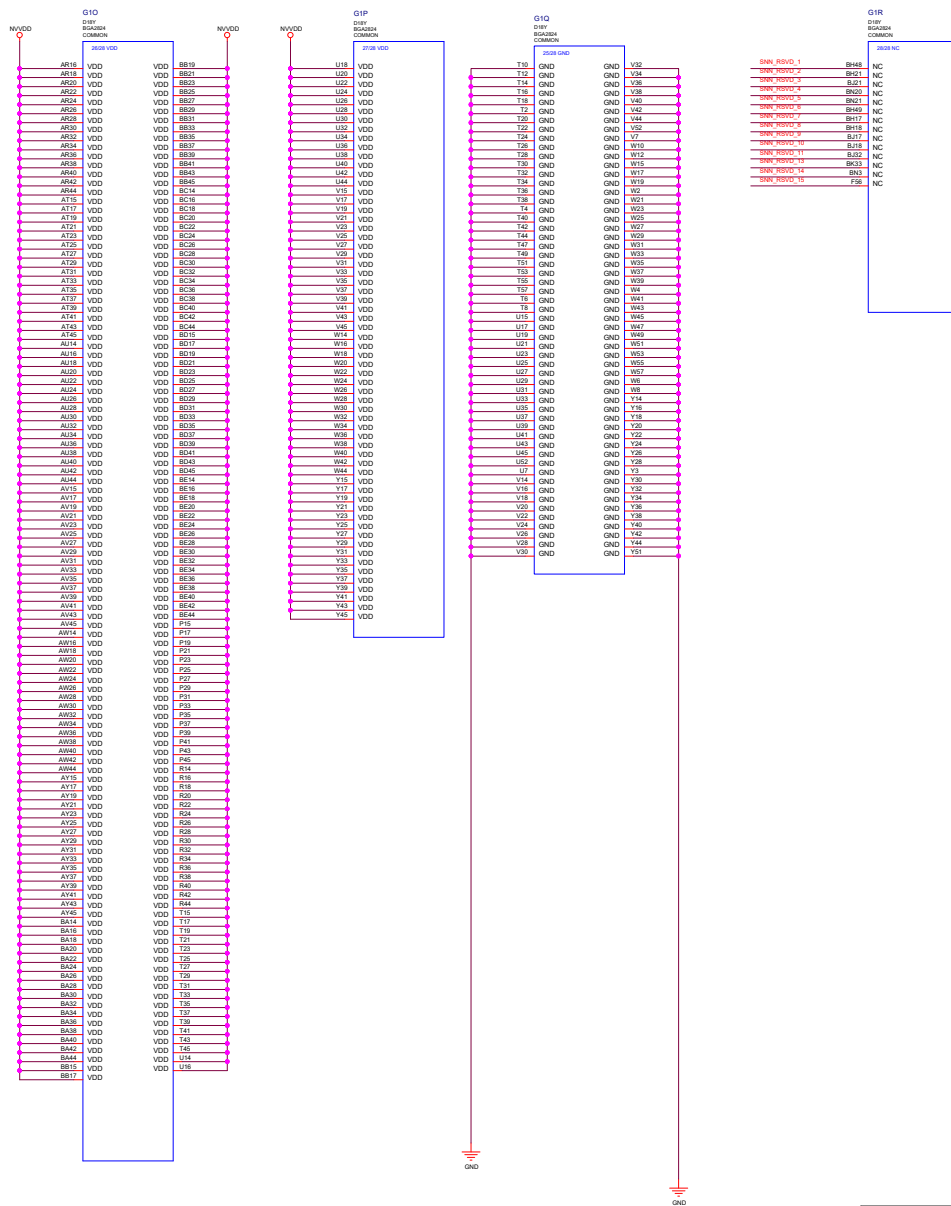
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GPU PWR and GND



GPU PWR GND NCs



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PAGE DETAIL	GPU PWR, GND and NCs

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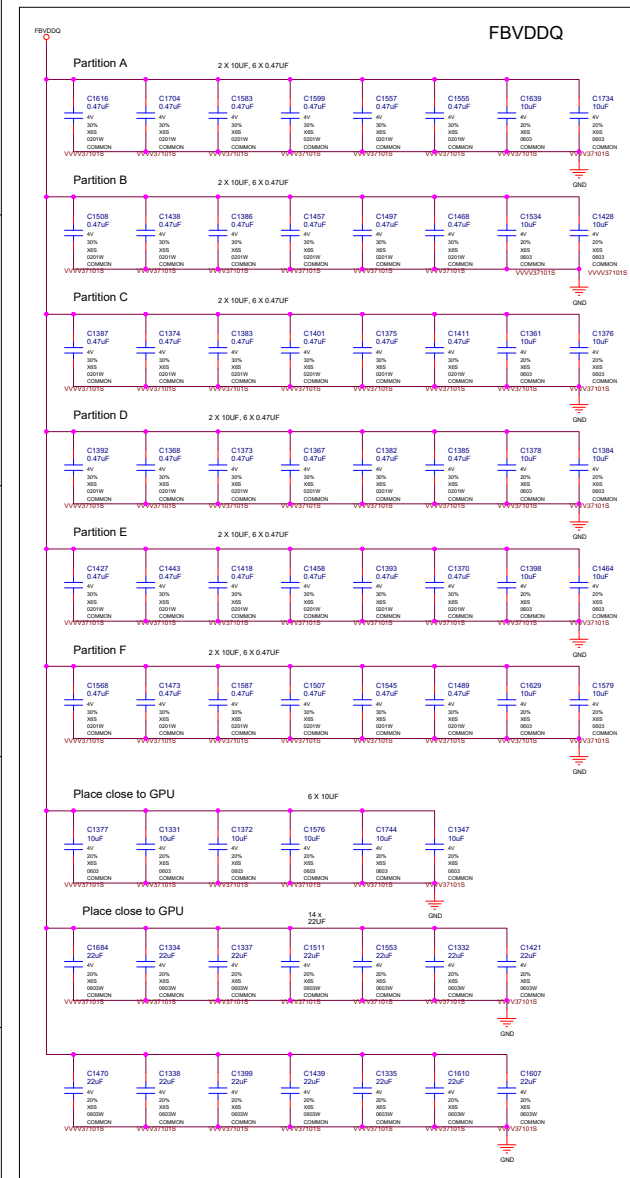
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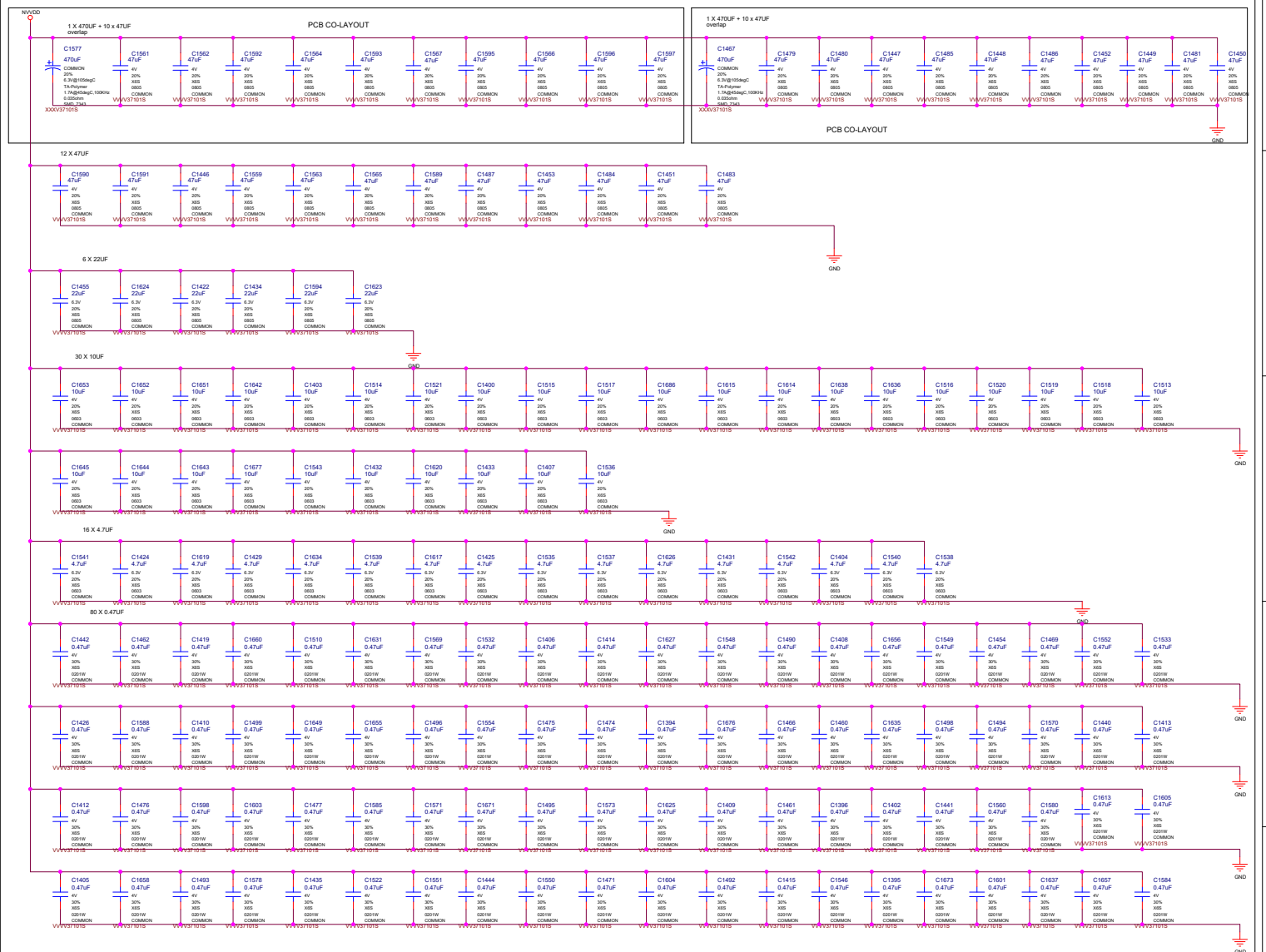
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GPU Decoupling



NVVDD



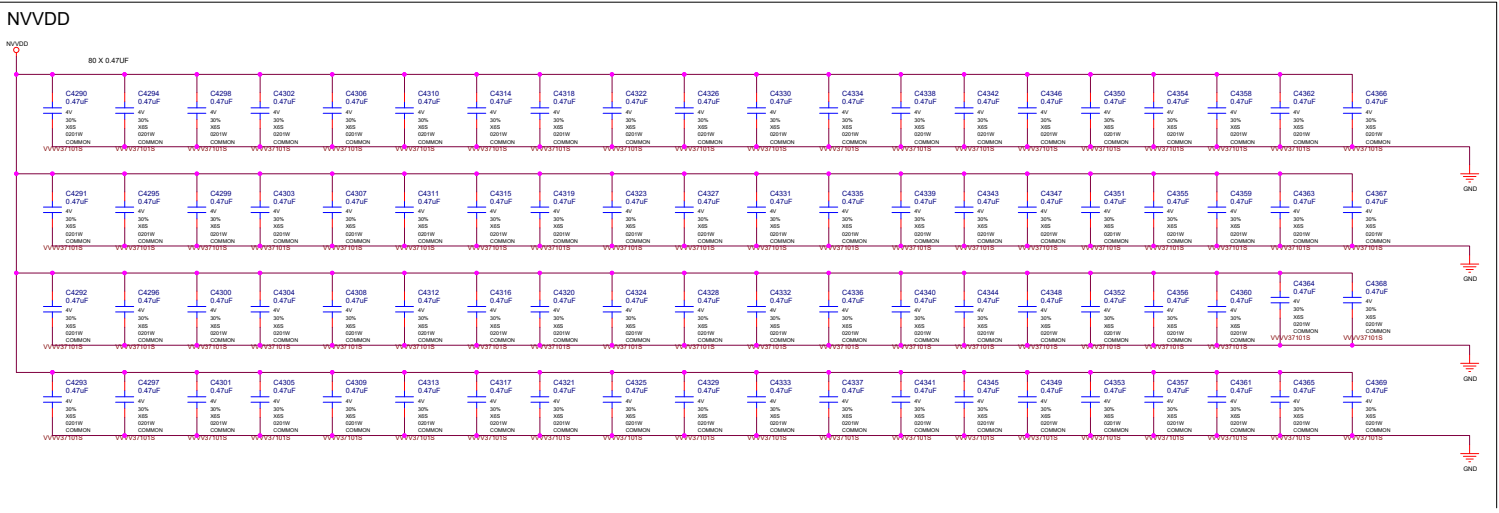
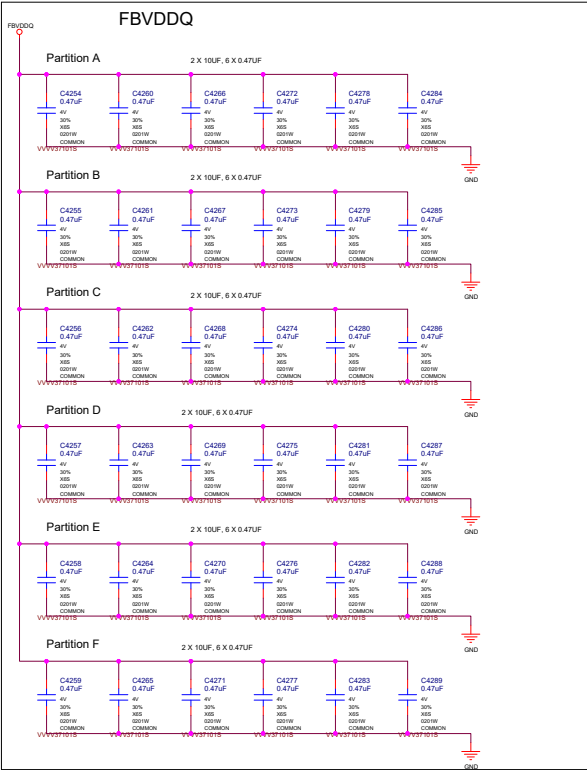
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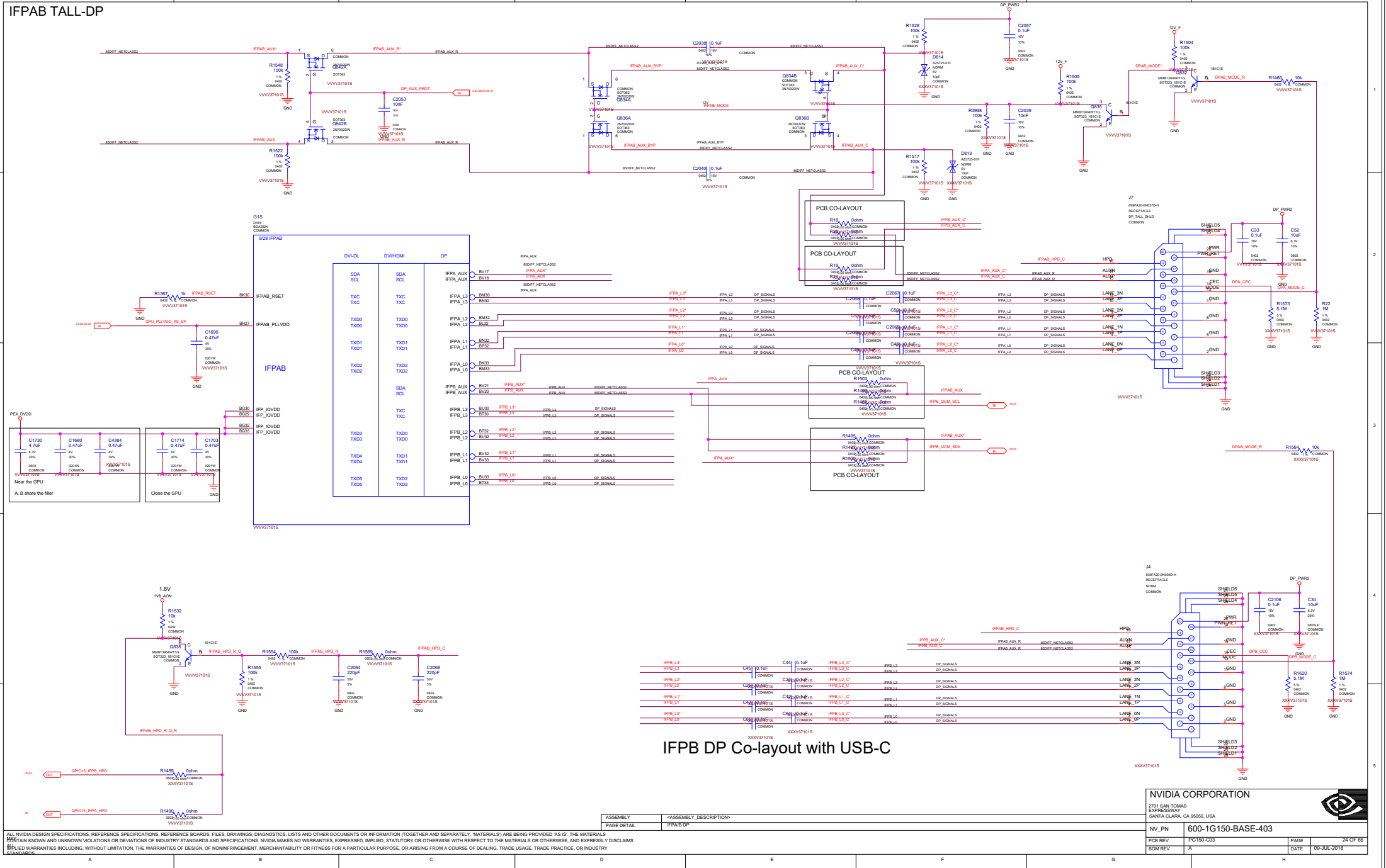


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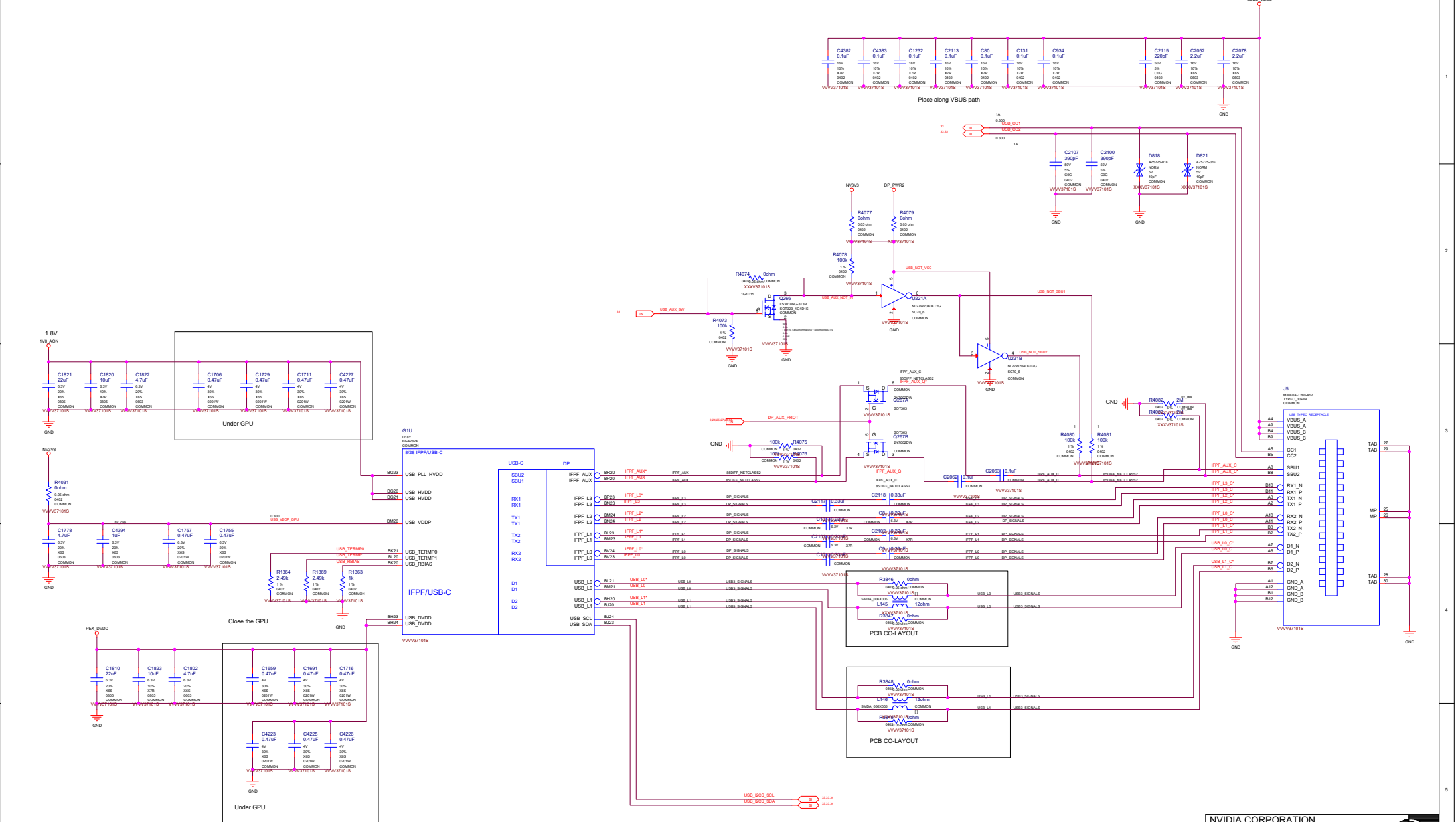
GPU Decoupling



IFPAB TALL-DP



IPFP USBC



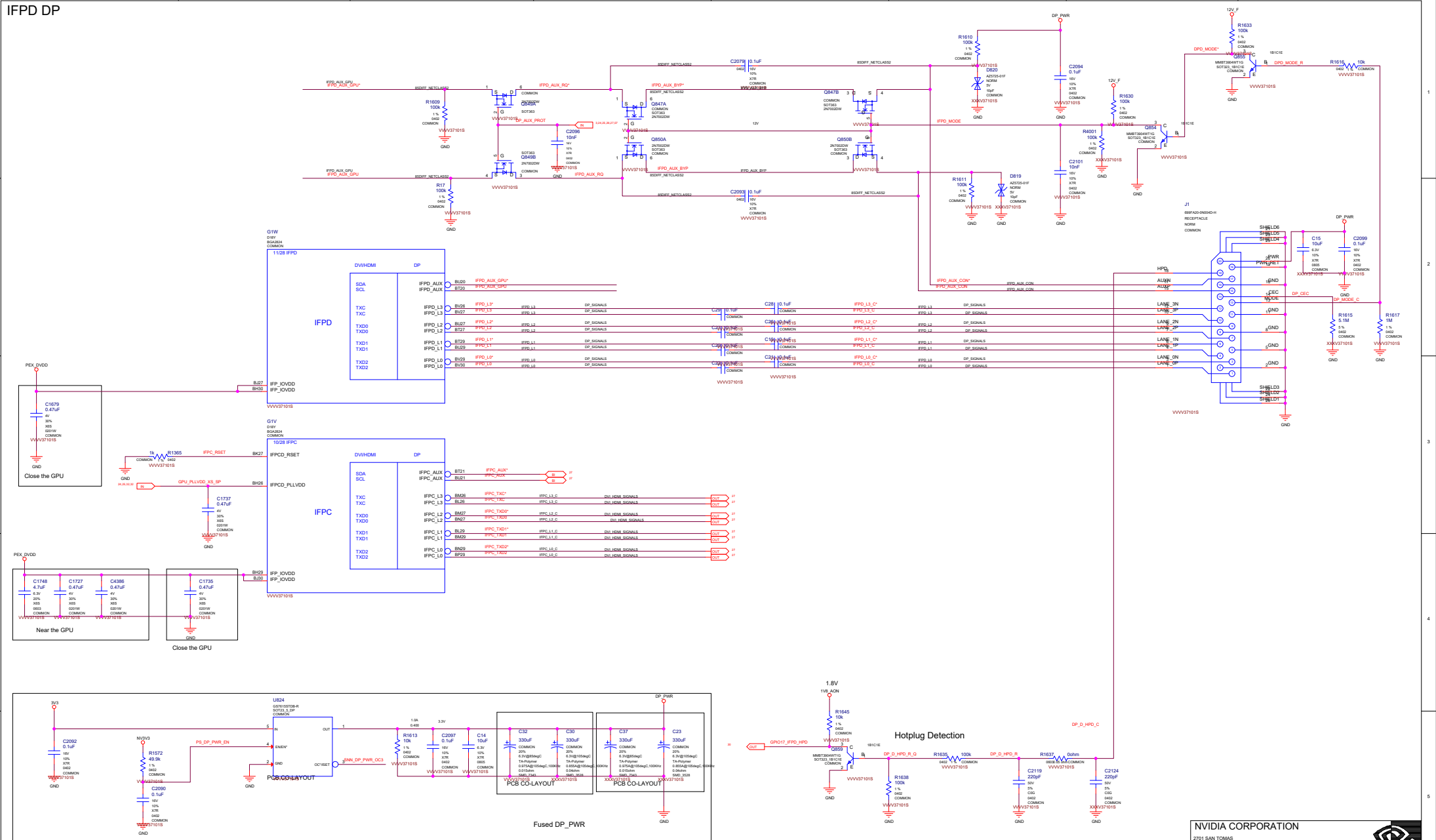
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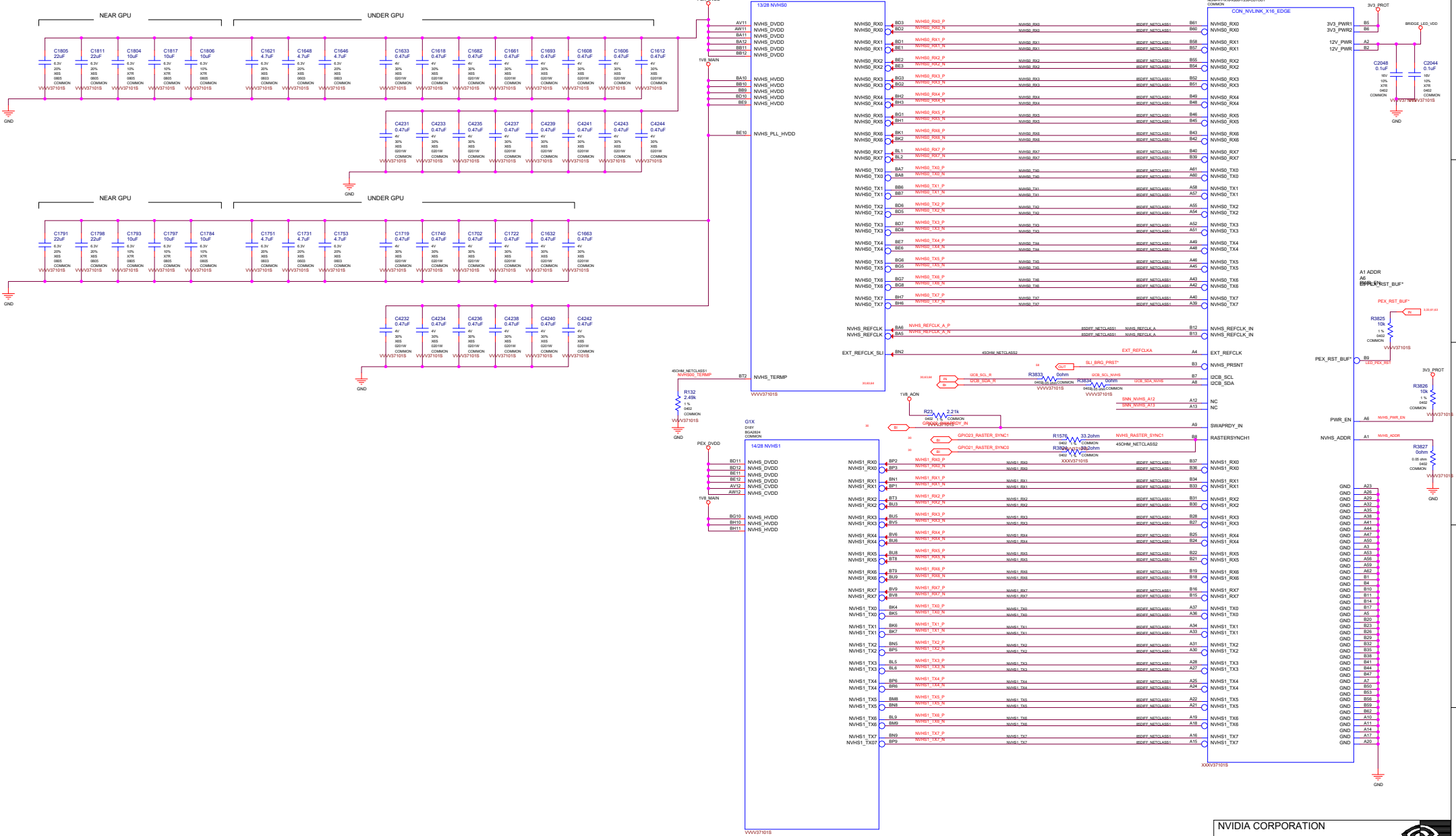
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IFPD DP



ASSEMBLY		PAGE DETAIL	
IFPD DP		IFPD DP	
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		DATE	09-JUL-2018

NVHS Interface and FRAME LOCK



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ASSEMBLY	<ASSEMBLY_DESCRIPTOR>
PAGE DETAIL	NVHS X16

NV PN	600-1G150-BASE-403
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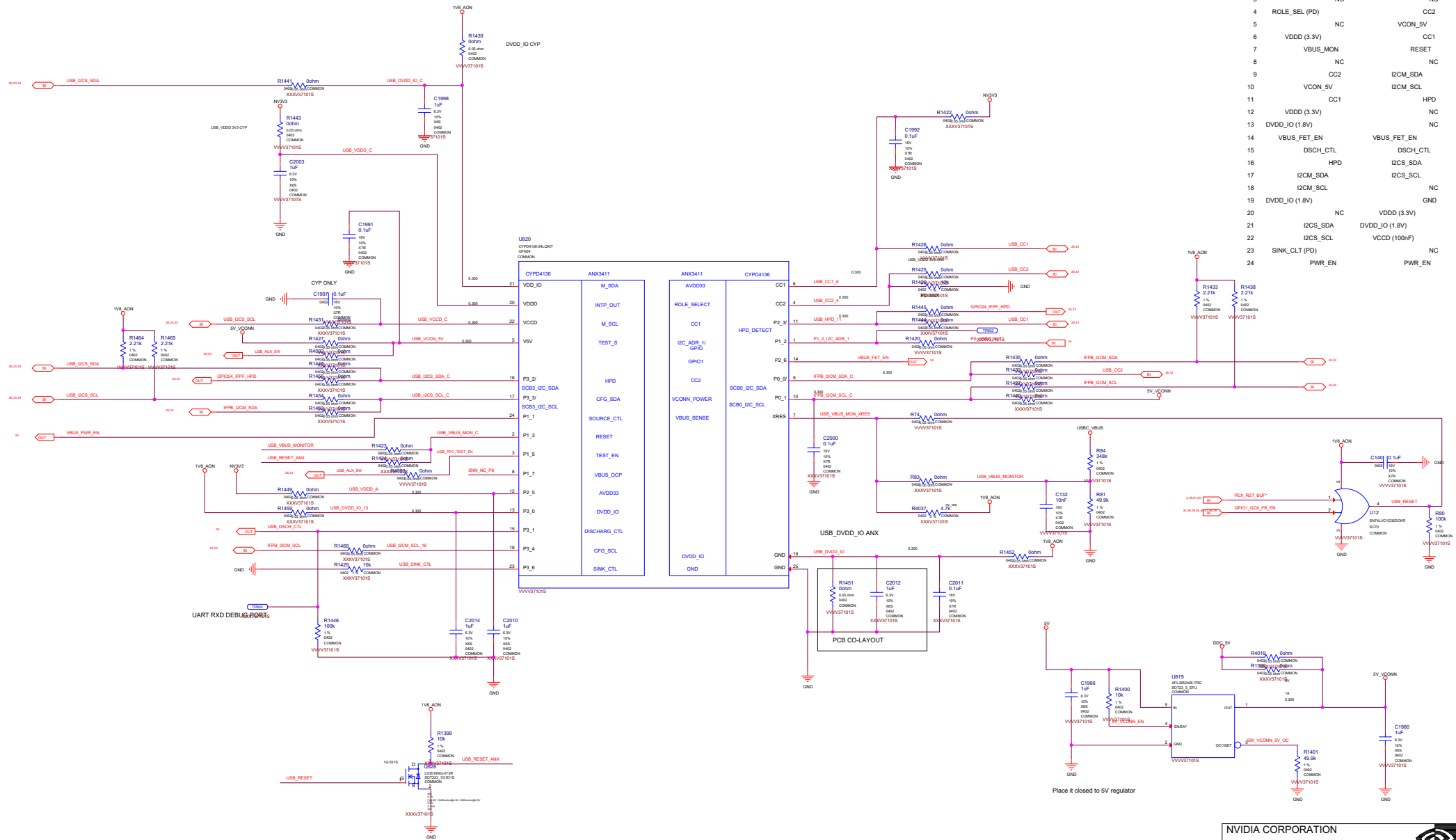
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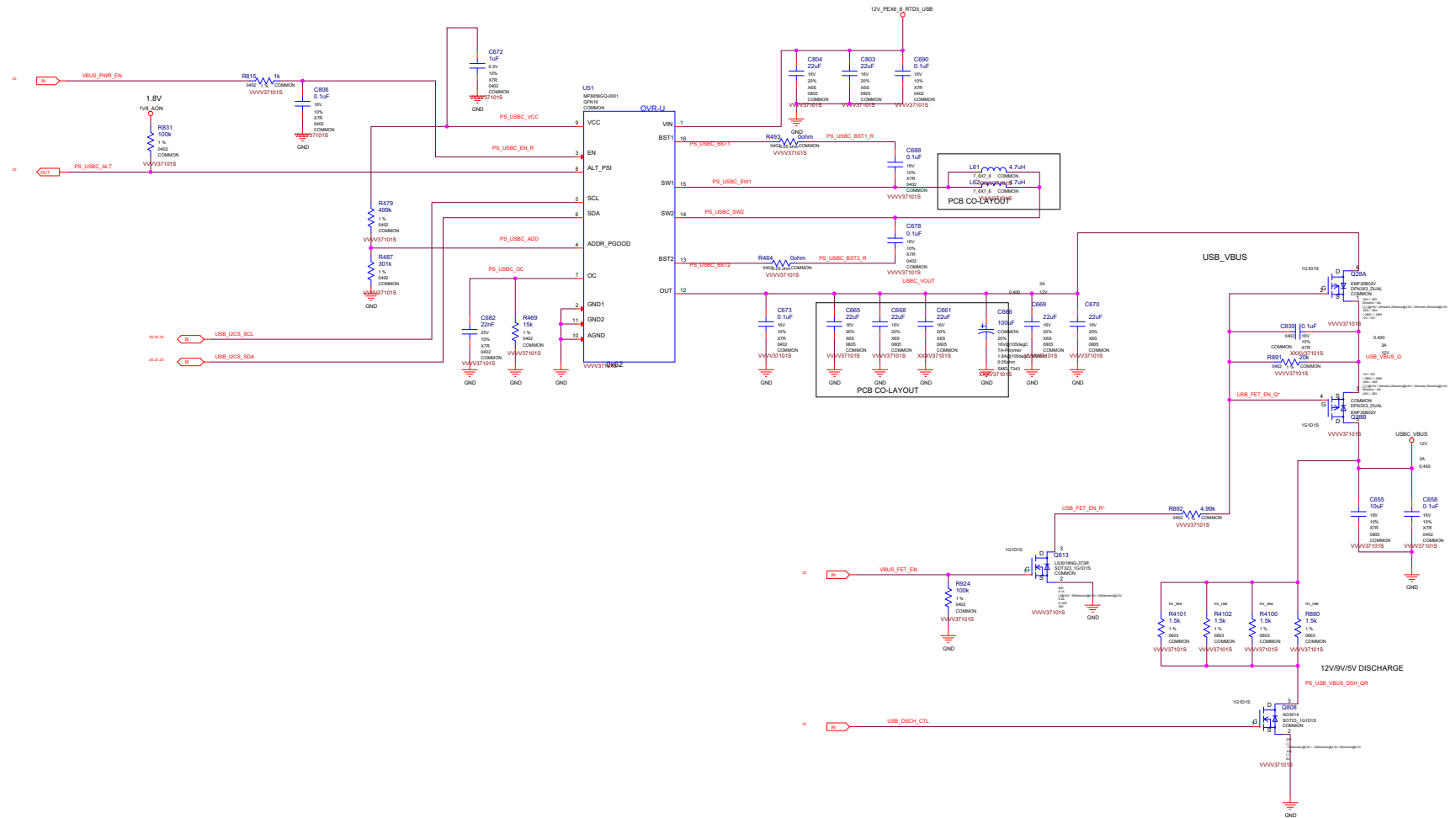
MISC: USB PPC



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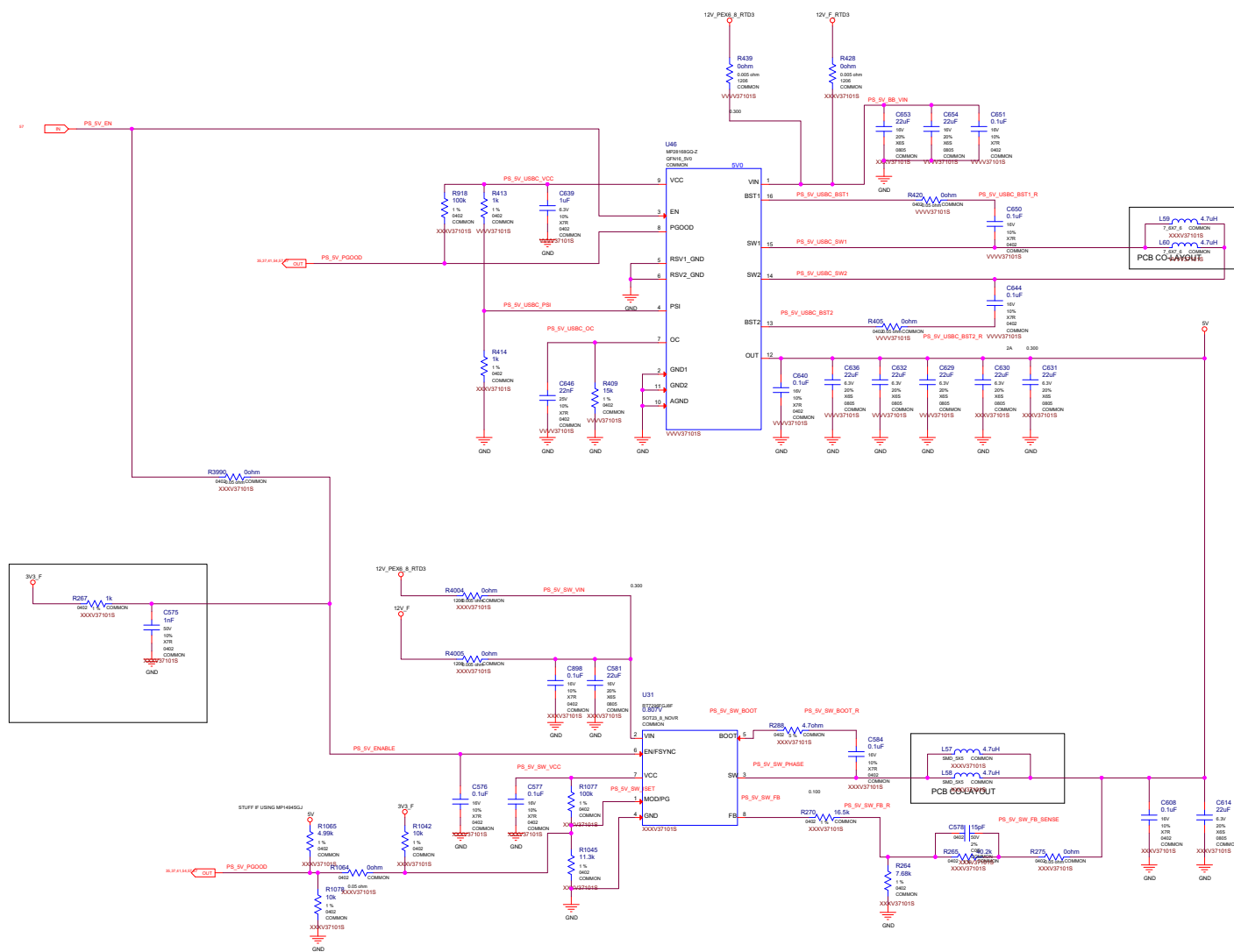
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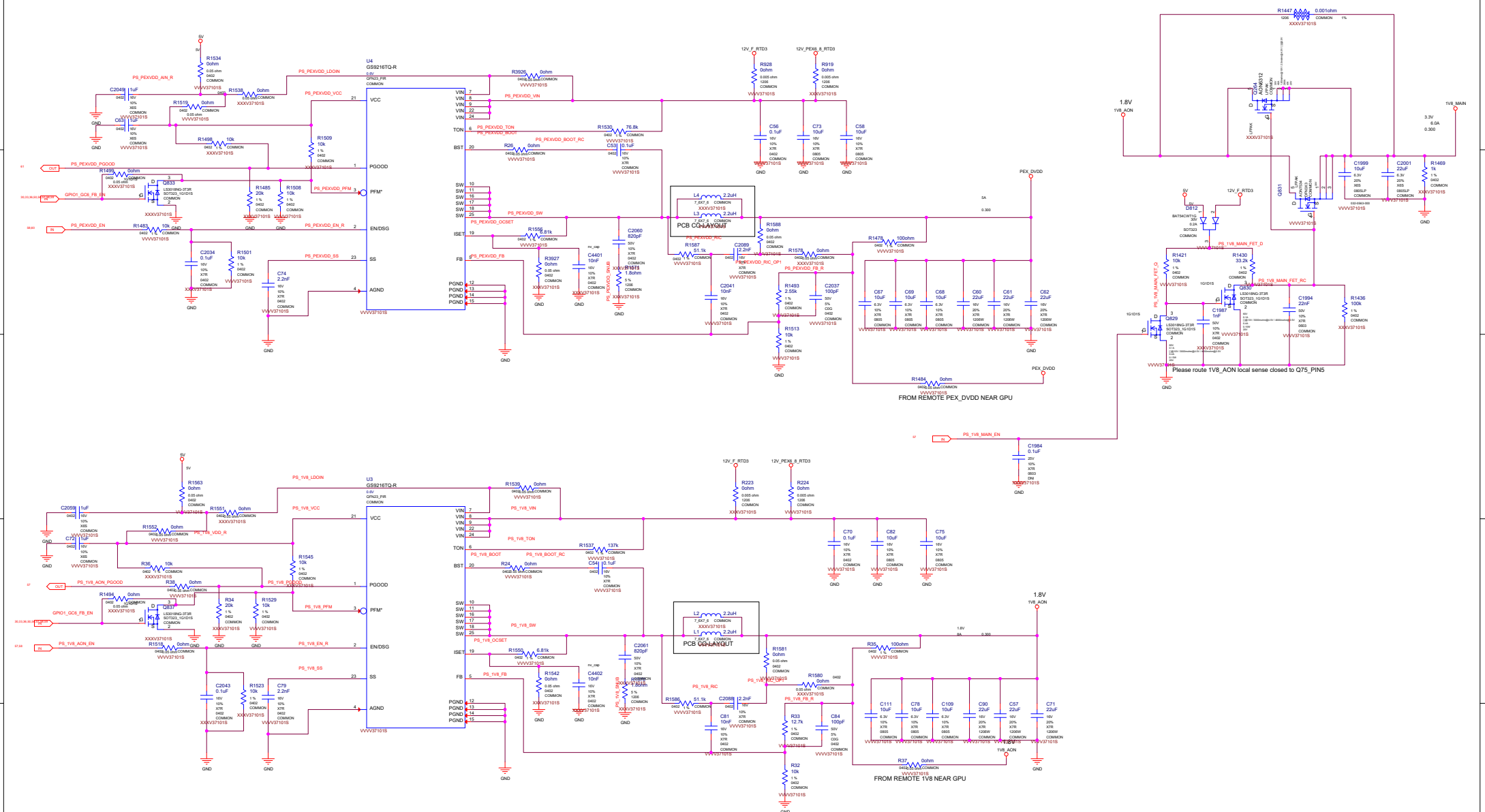


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PS: PEXVDD 1V8 Rail



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ASSEMBLY		"ASSEMBLY DESCRIPTION"		EXPRESSWAY SANTA CLARA, CA 95050, USA	
PAGE DETAIL		PS: PEXVDD 1V8 Rail		600-1G150-BASE-403	
RAILS		NV_PN		38 OF 56	
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ISTORY		BOM REV		DATE	
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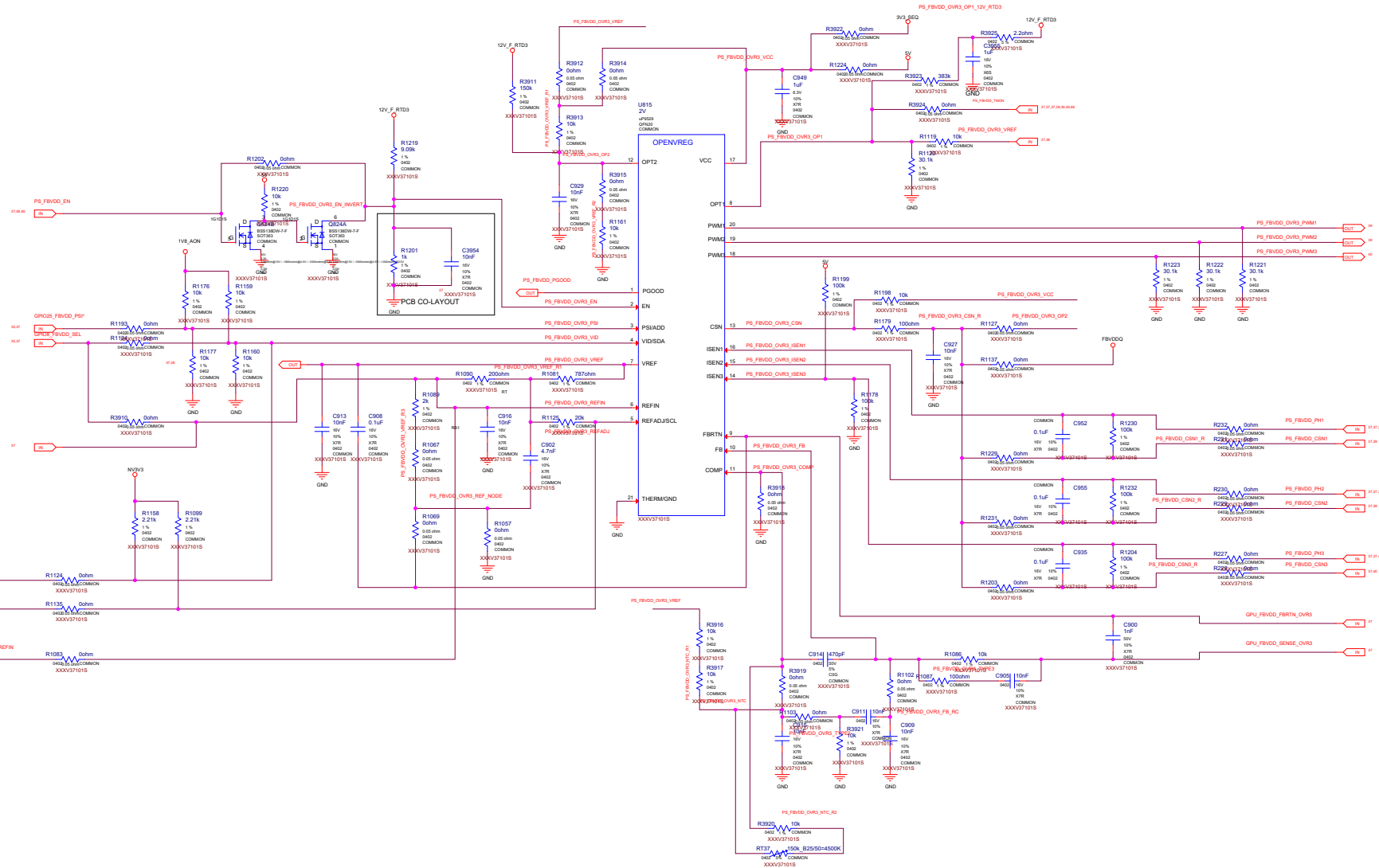
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RESULTS



PS: FBVDD Controller OVR3



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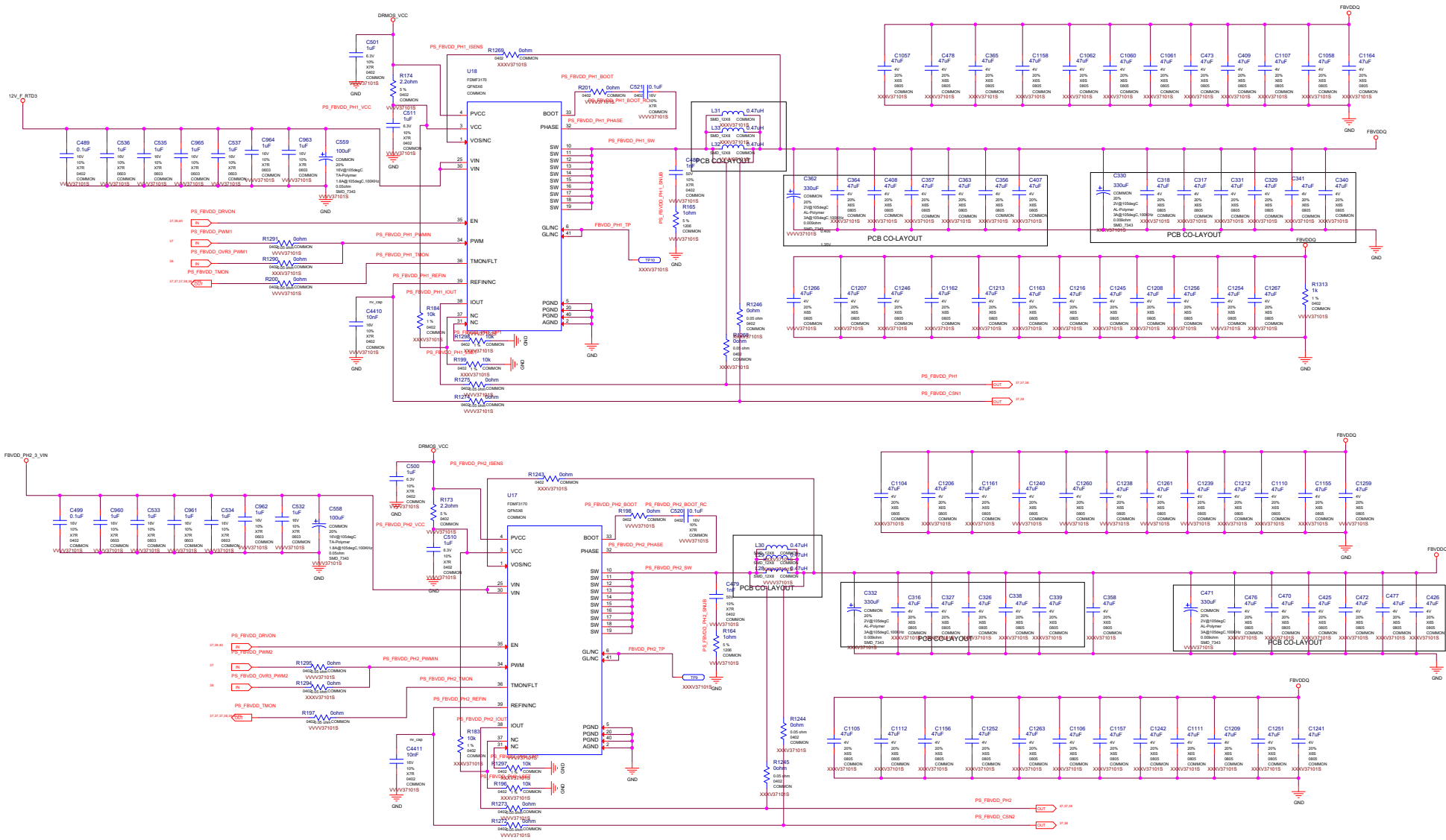
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PAGE DETAIL	PS: FBVDD Controller OVR3



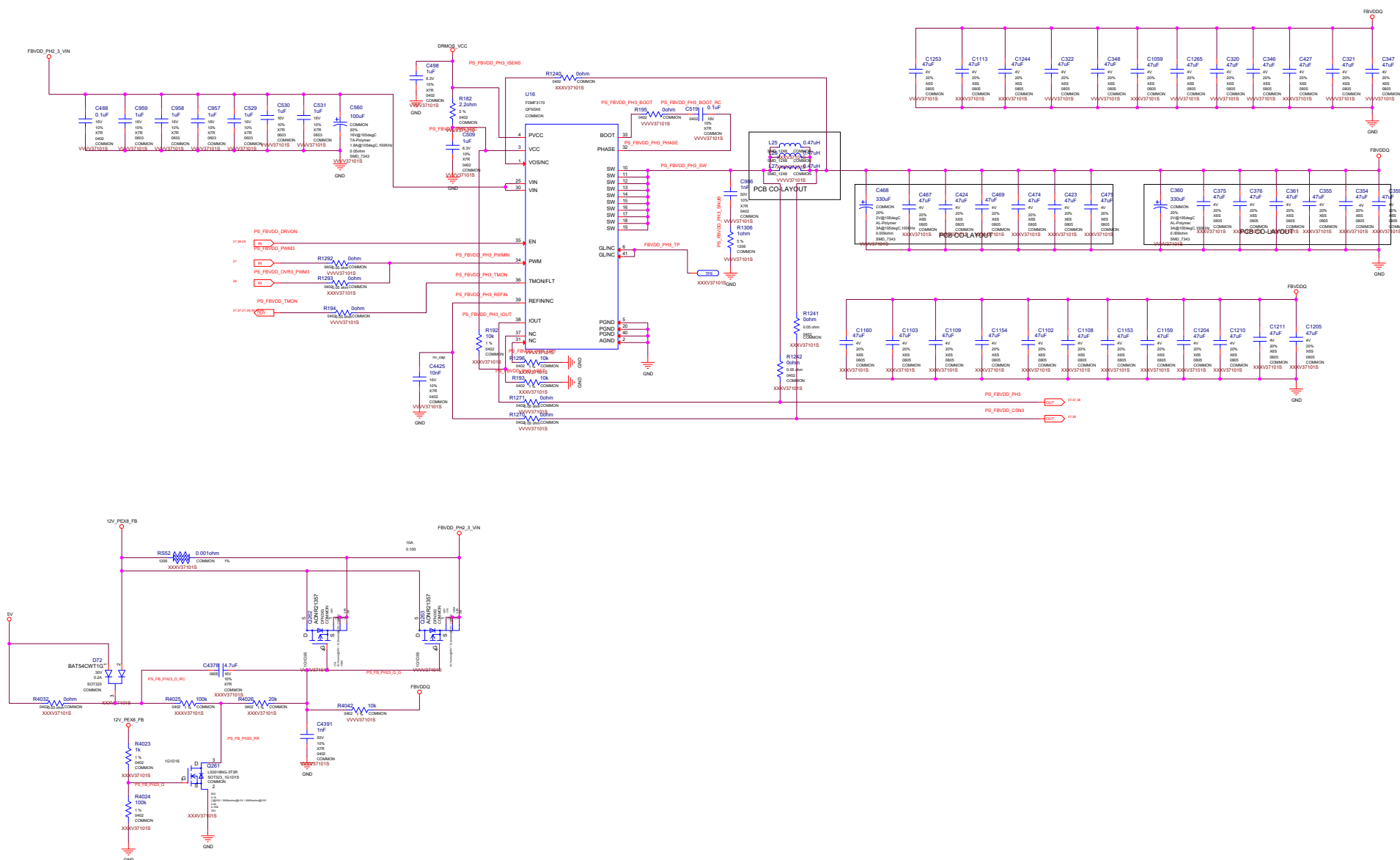
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PS: FBVDD PH3



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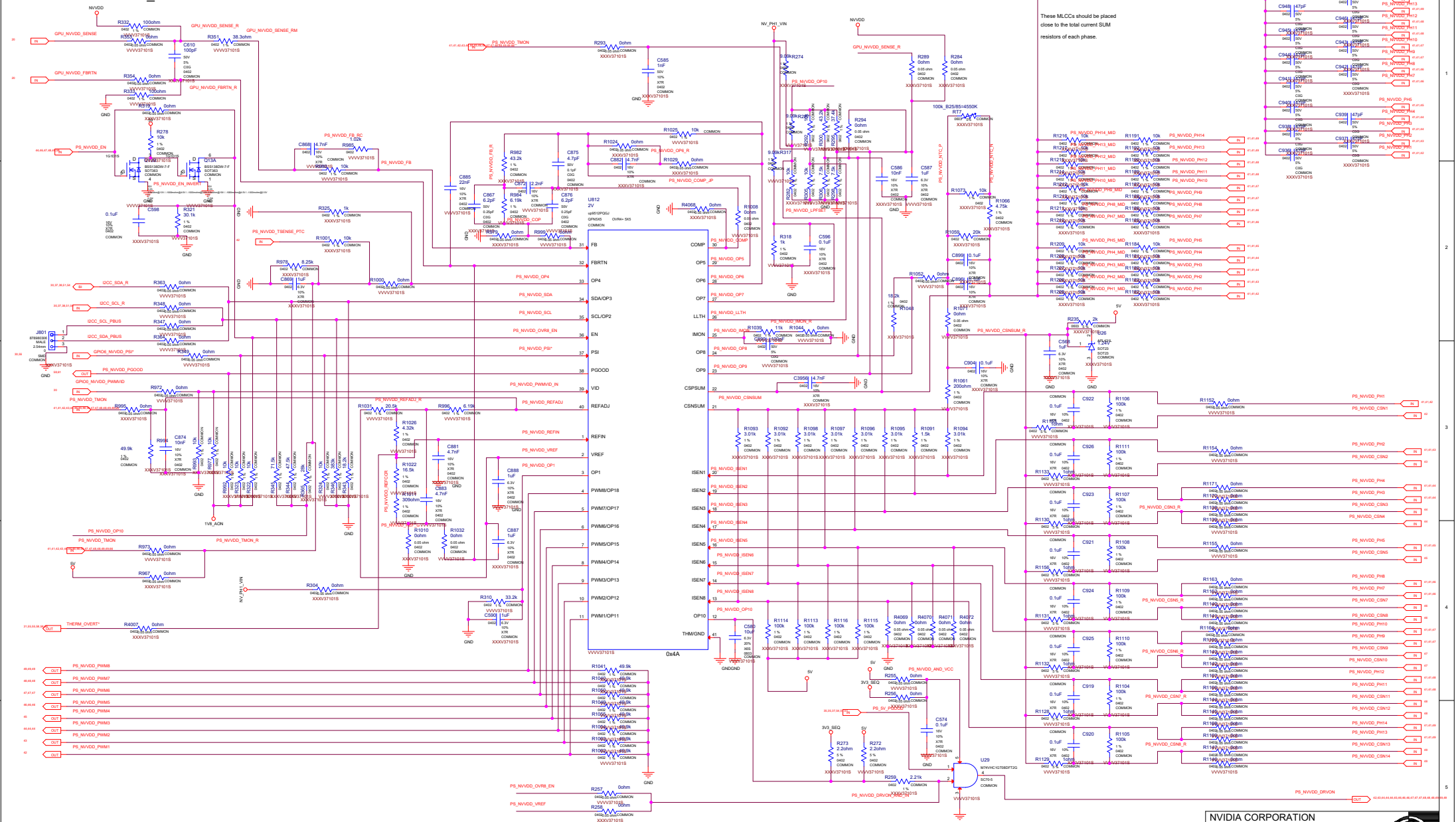


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PS: NVVDD Controller_OVR8



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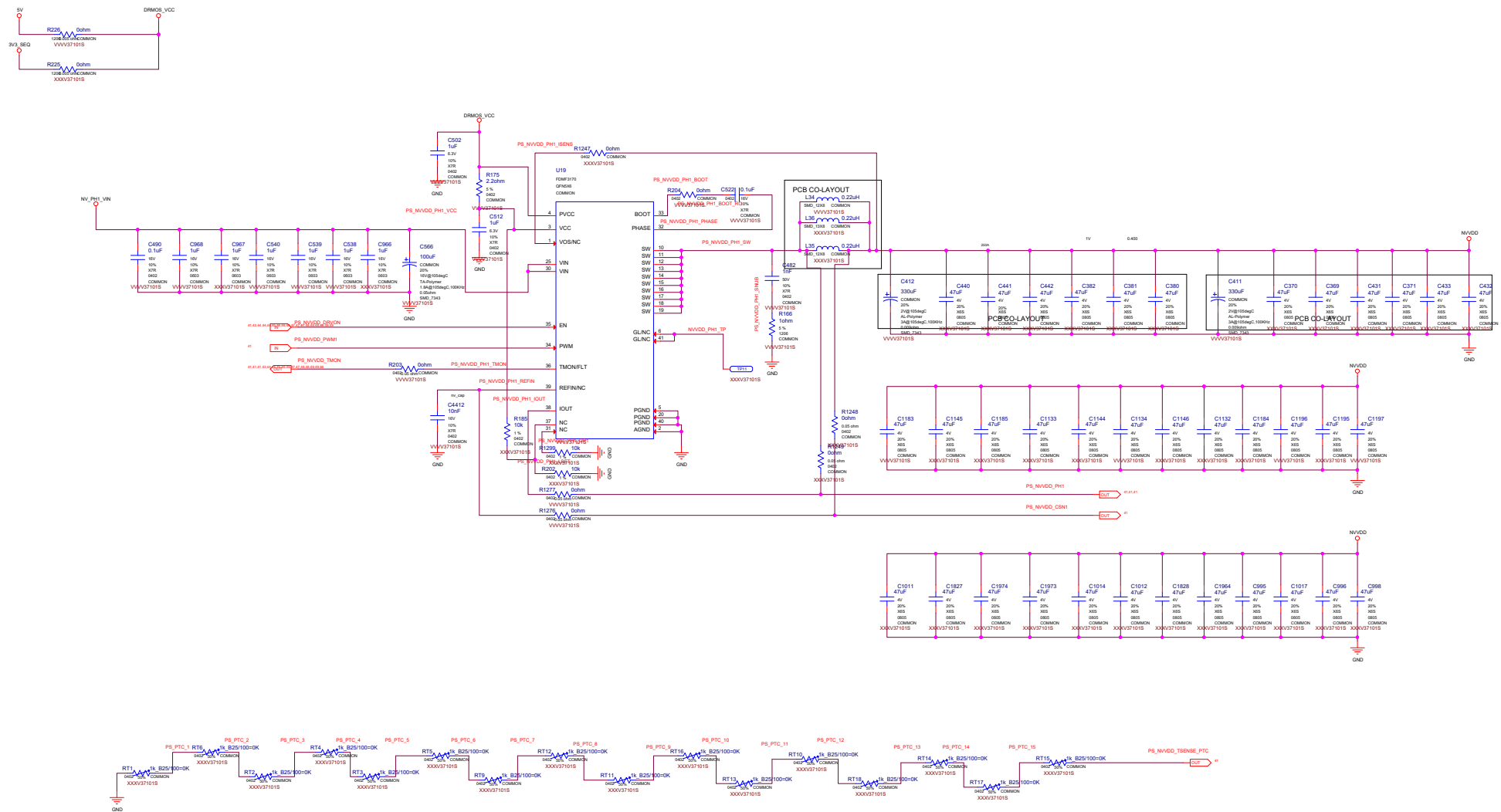
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PAGE DETAIL	PS: NVVDD Controller_OVR8

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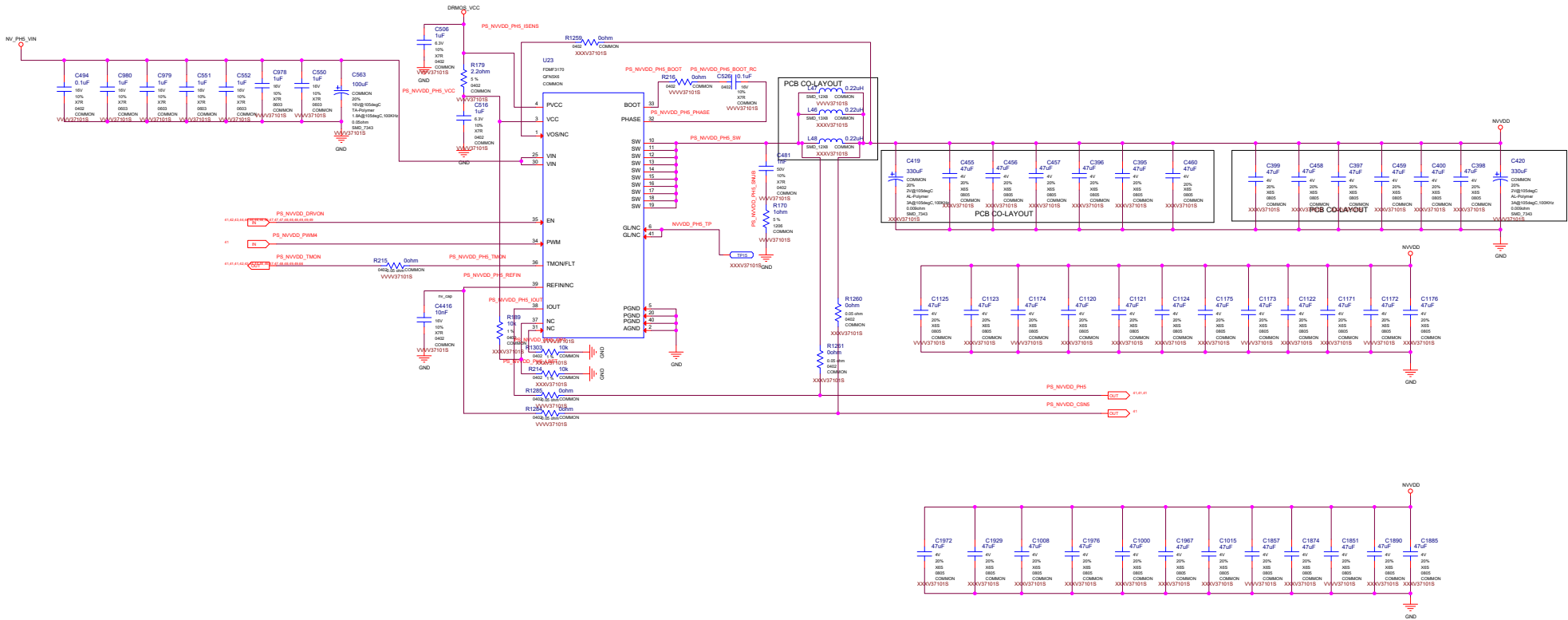
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PS: NVVDD Phase 5



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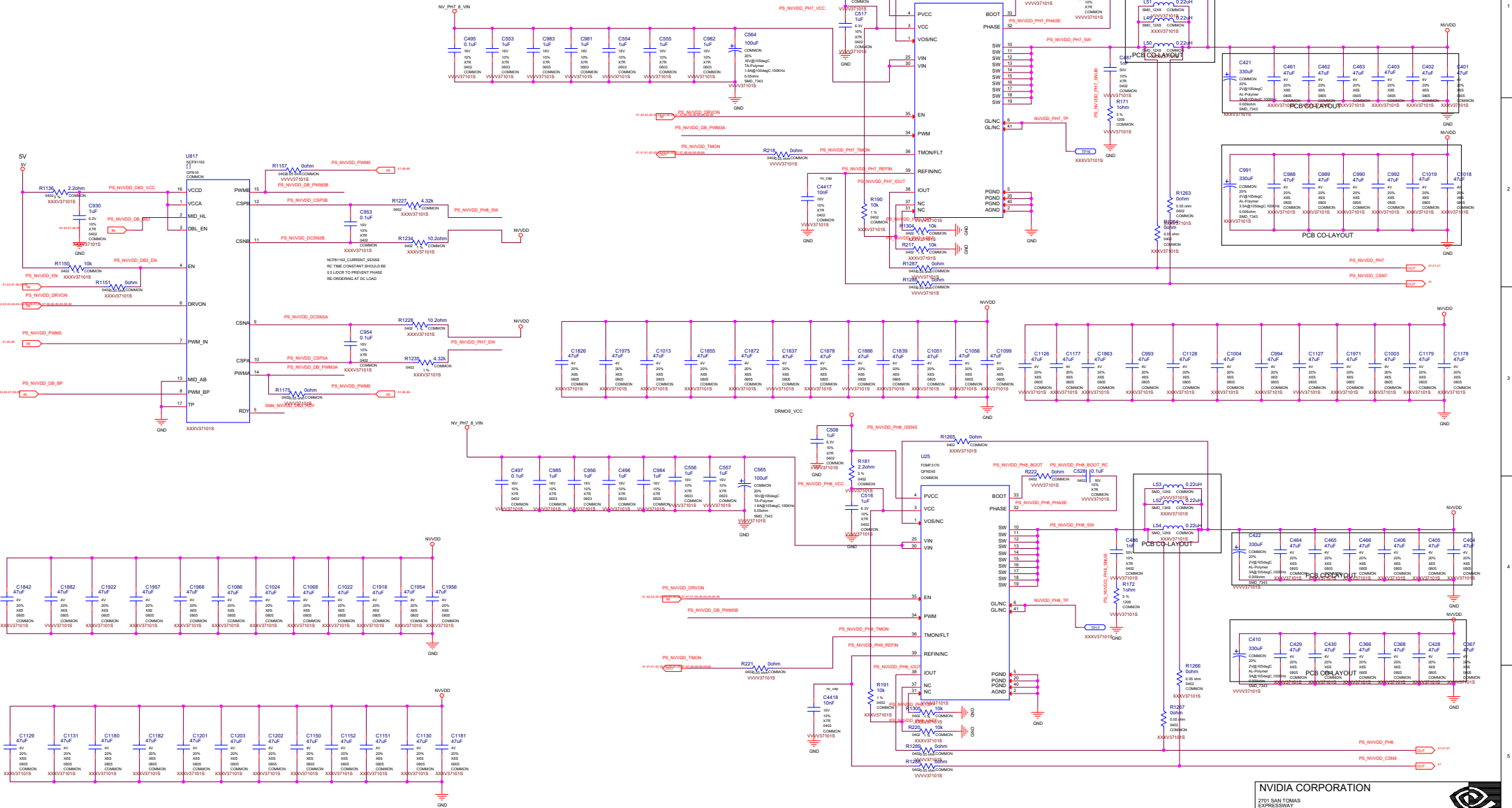
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PAGE DETAIL	PS: NVVDD Phase 5

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ASSEMBLY		*ASSEMBLY DESCRIPTION*	
PAGE DETAIL		PS: NVVDD Phase 7, 8	

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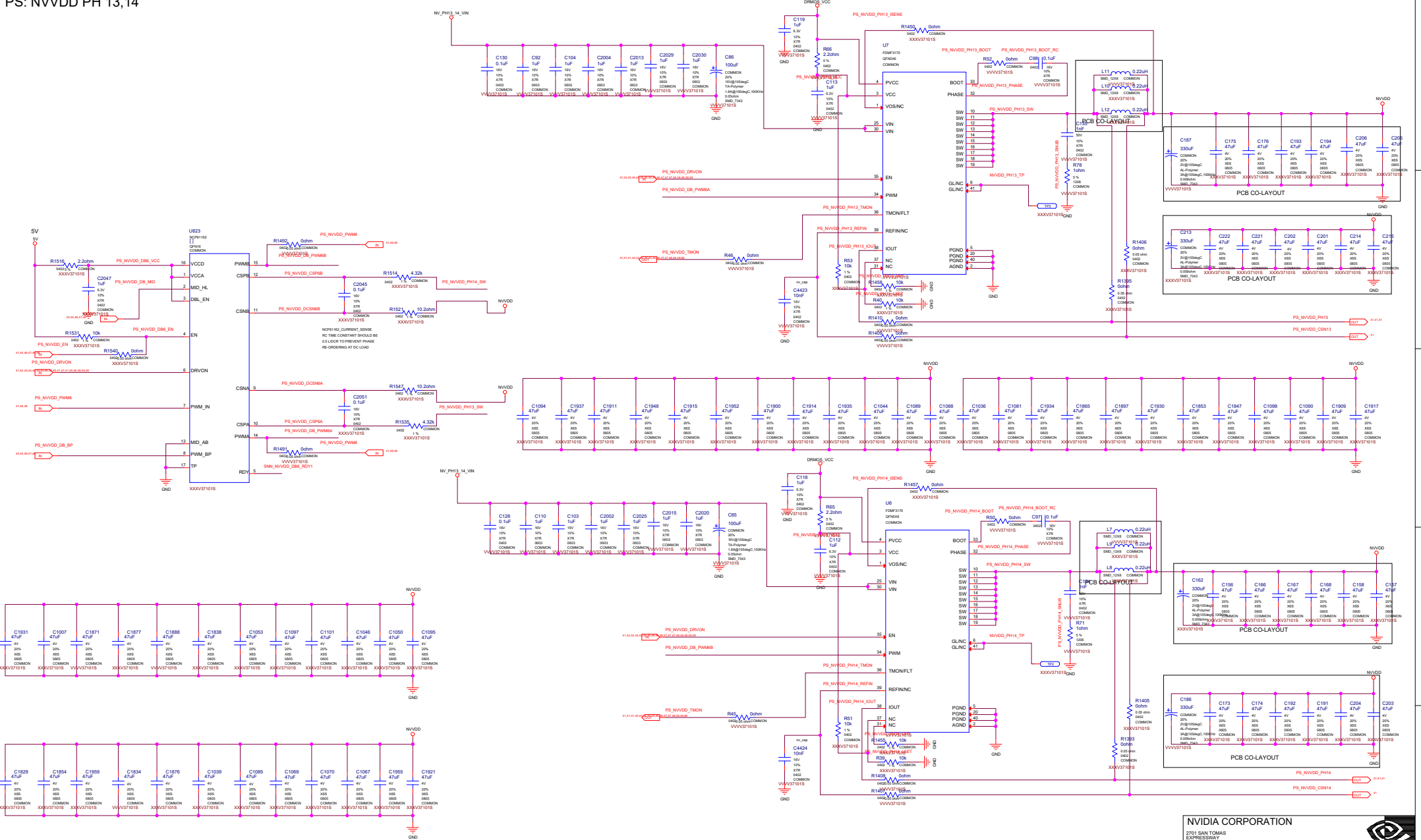
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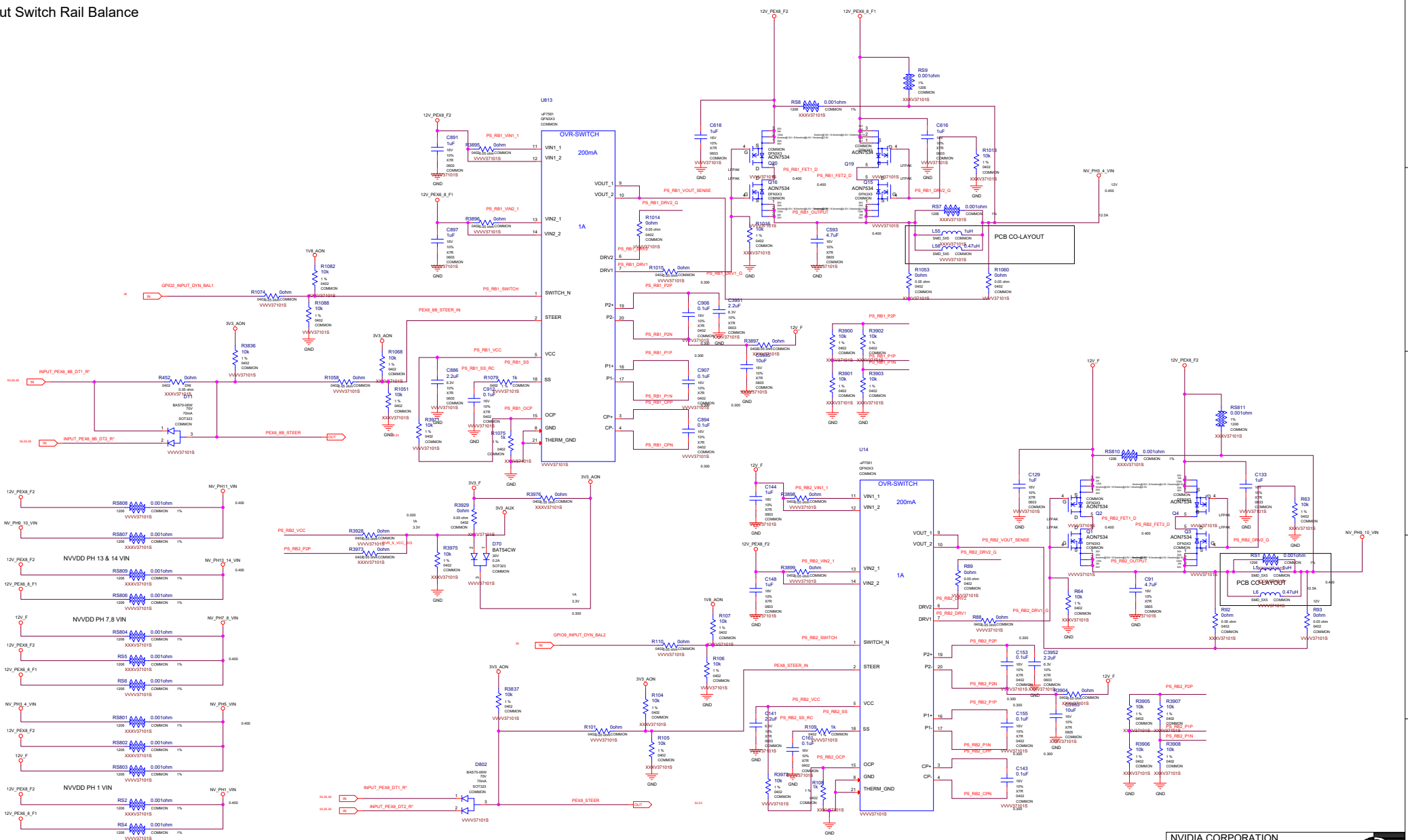
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PS: Input Switch Rail Balance



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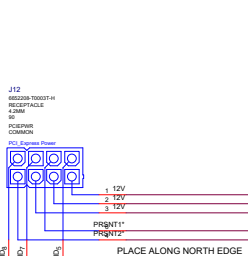
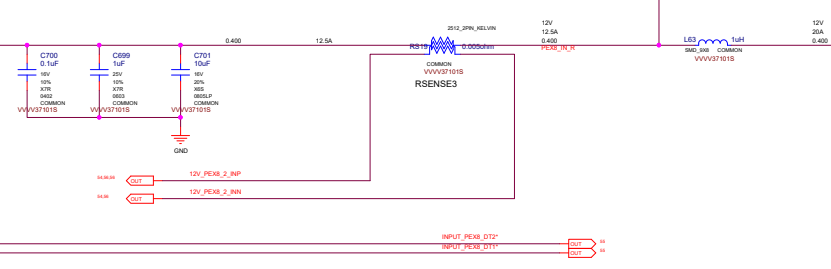
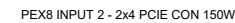
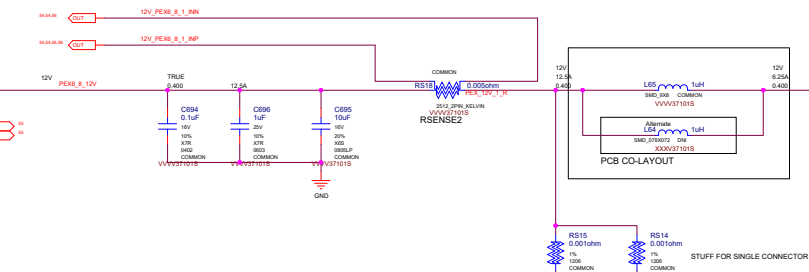
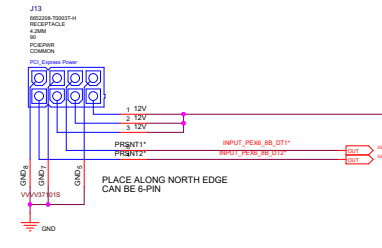
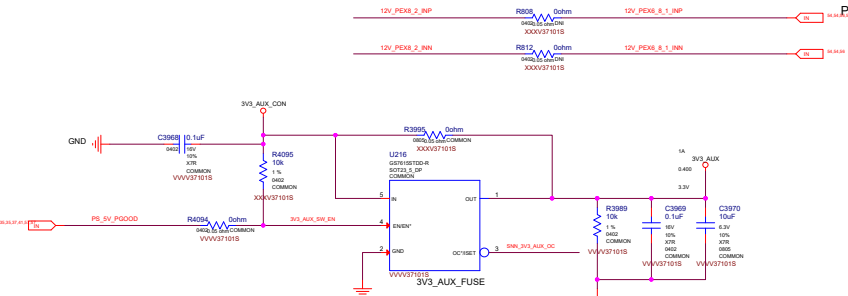
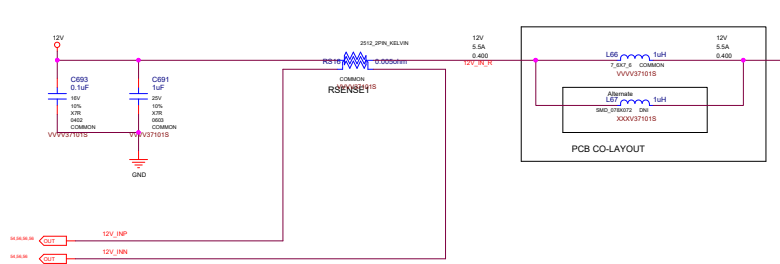
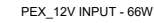
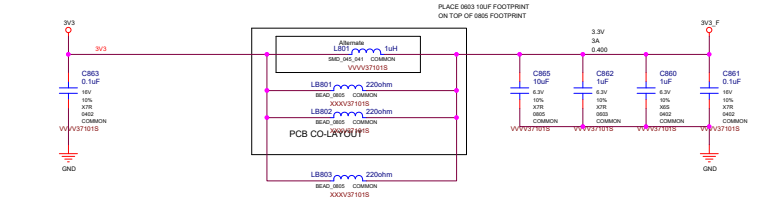
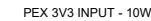
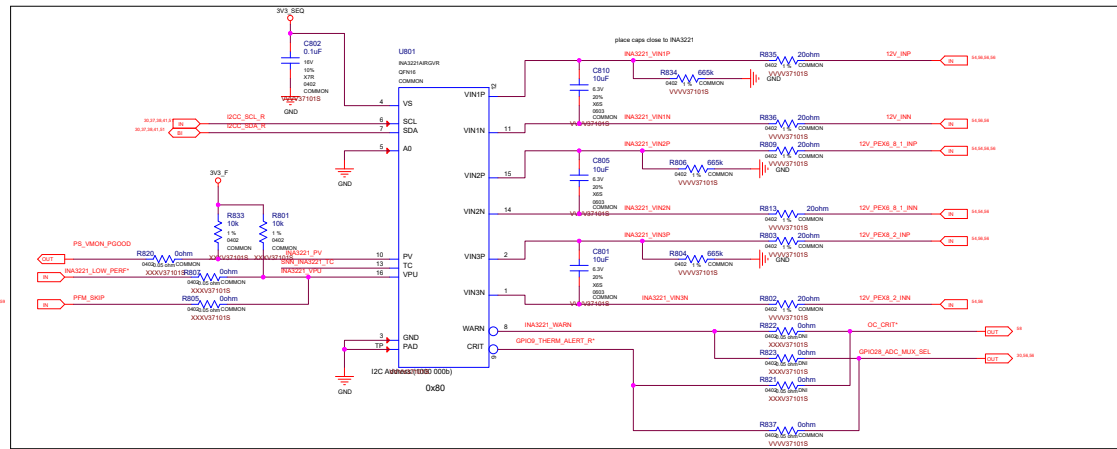
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PS: Inputs, Filtering, and Monitoring



ASSEMBLY	<ASSEMBLY_DESCRIPTION>
PAGE DETAIL	PS: Input, filtering, and Monitoring

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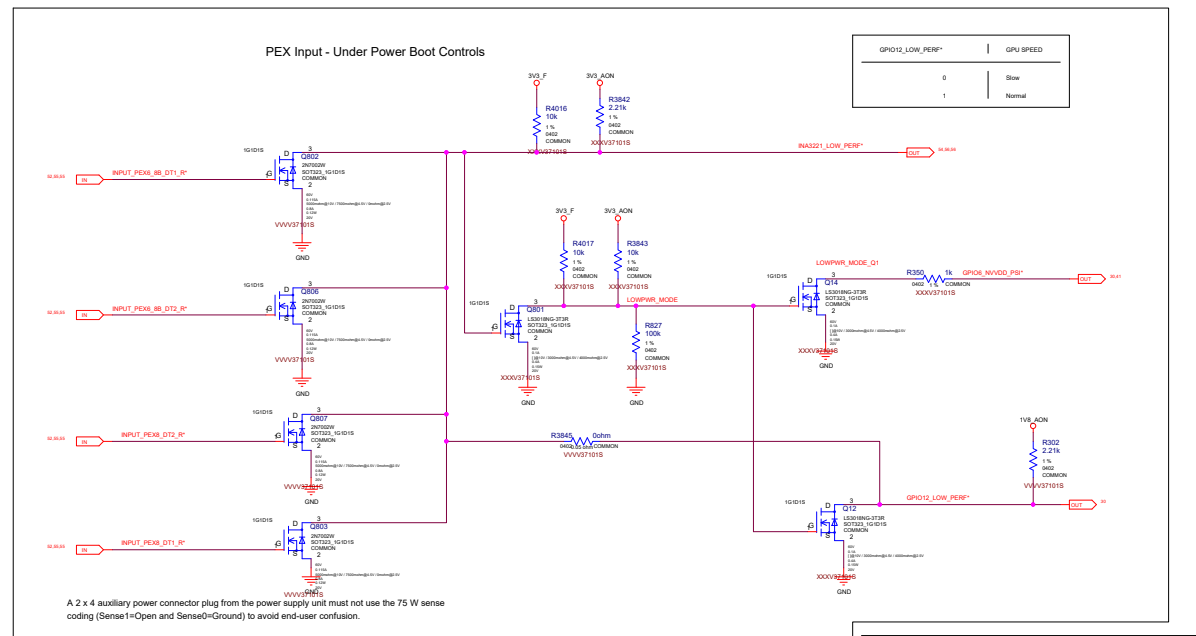
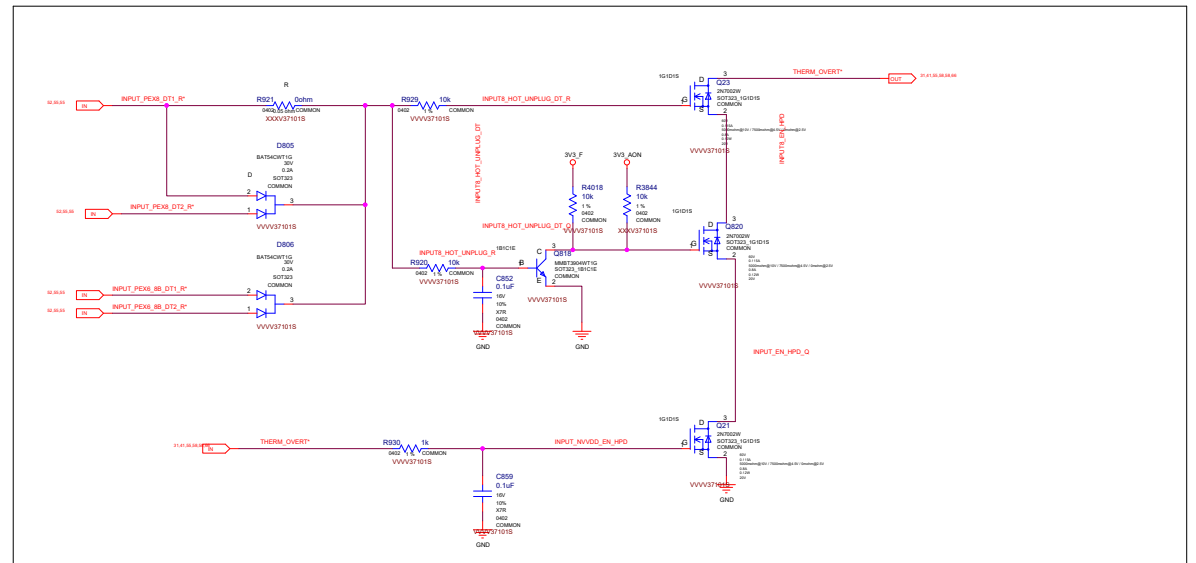
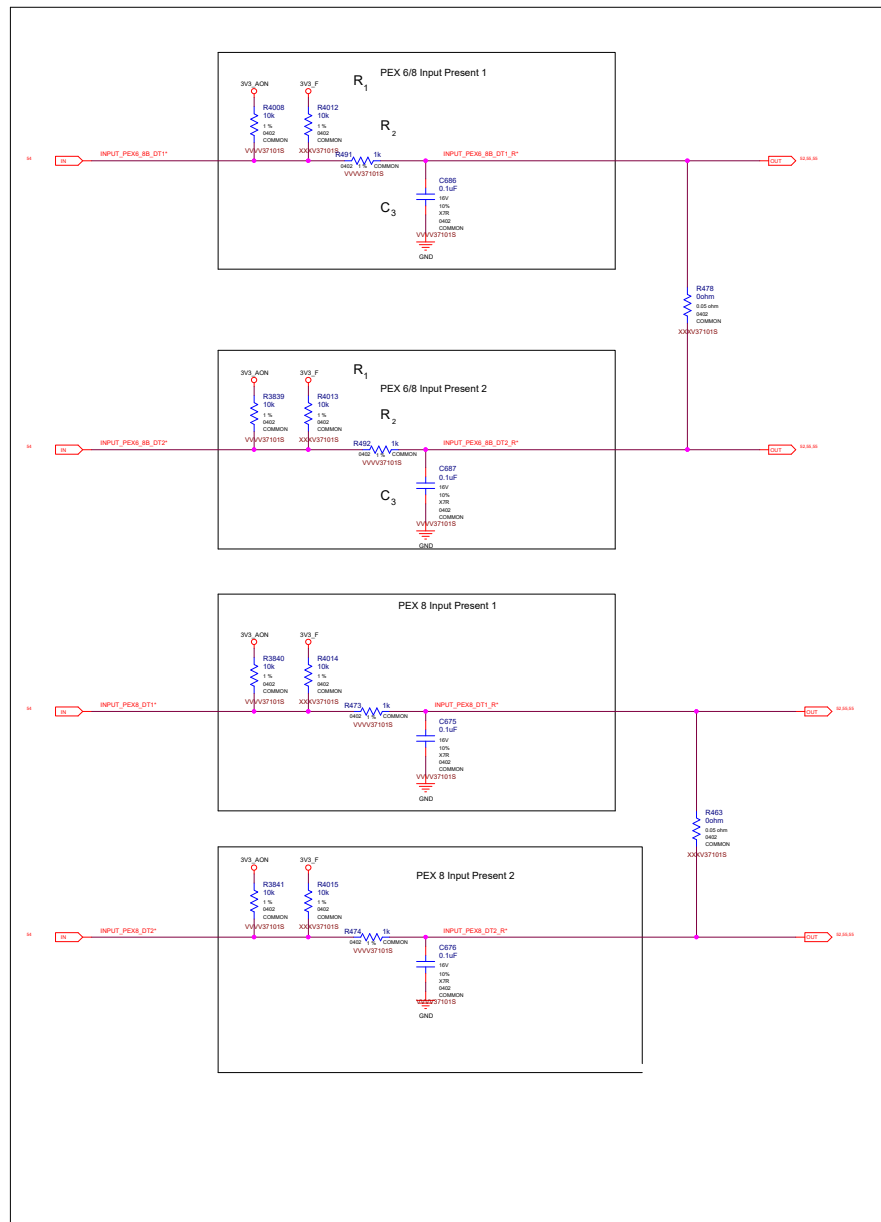


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PS: 12V Current Steering & Hot Unplug Detect



ASSEMBLY	<ASSEMBLY_DESCRIPTION>
PAGE DETAIL	PS: Current Storing, Hot Unplug

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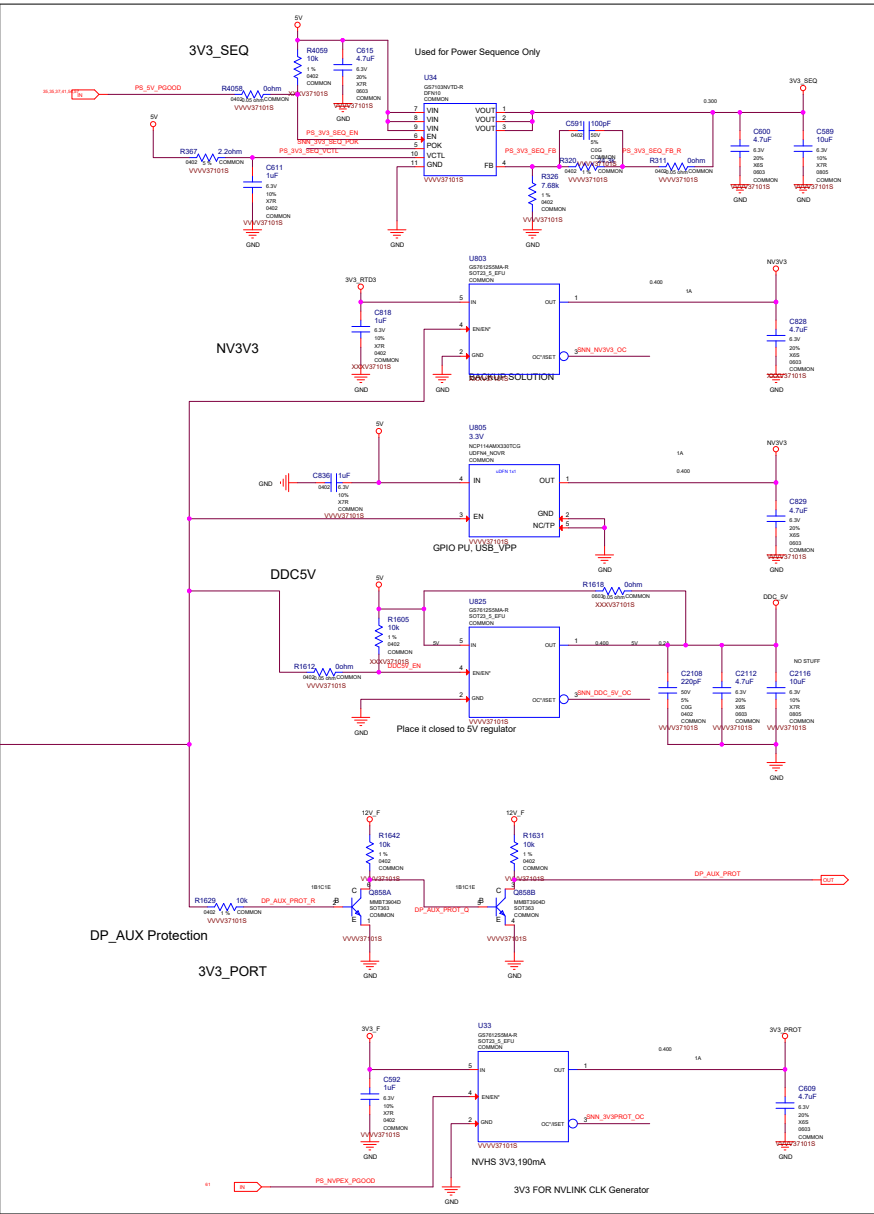
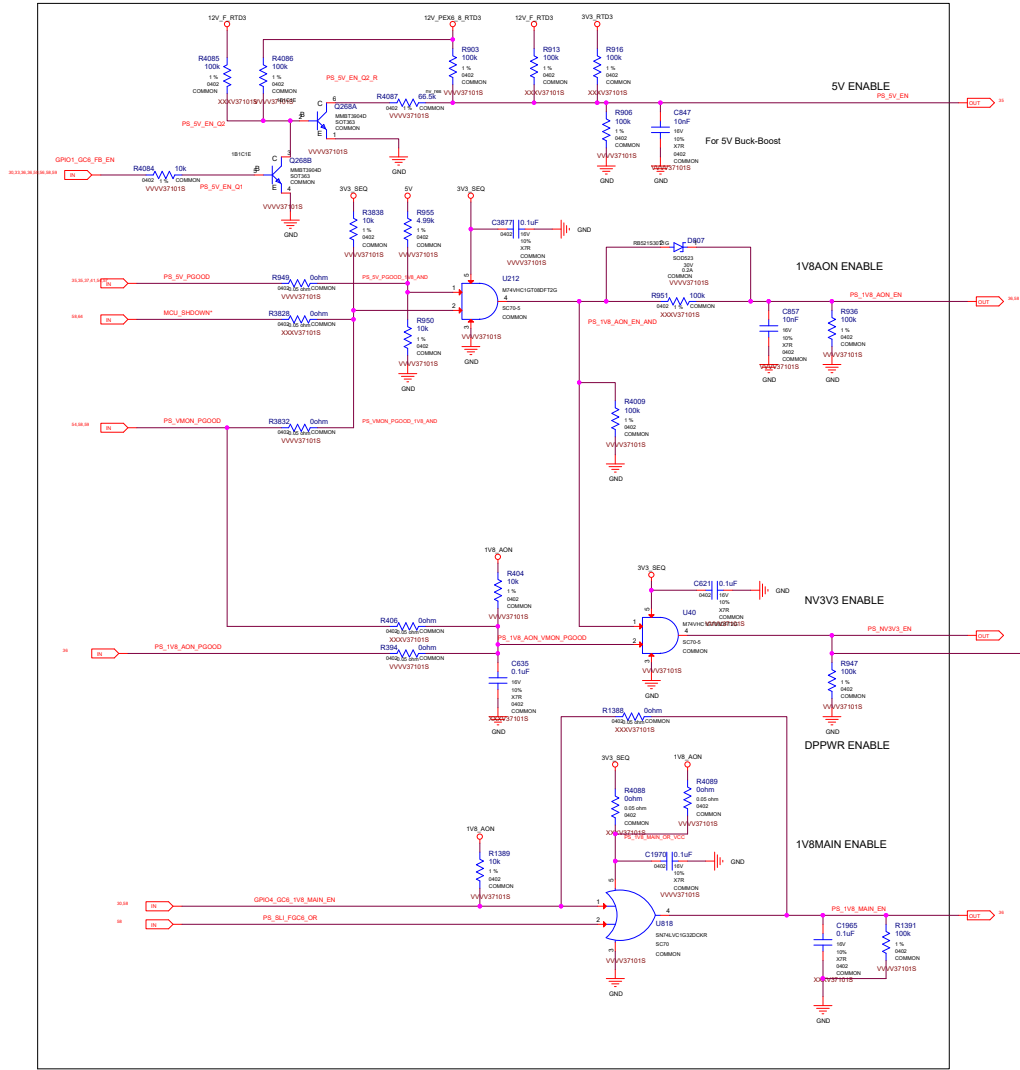
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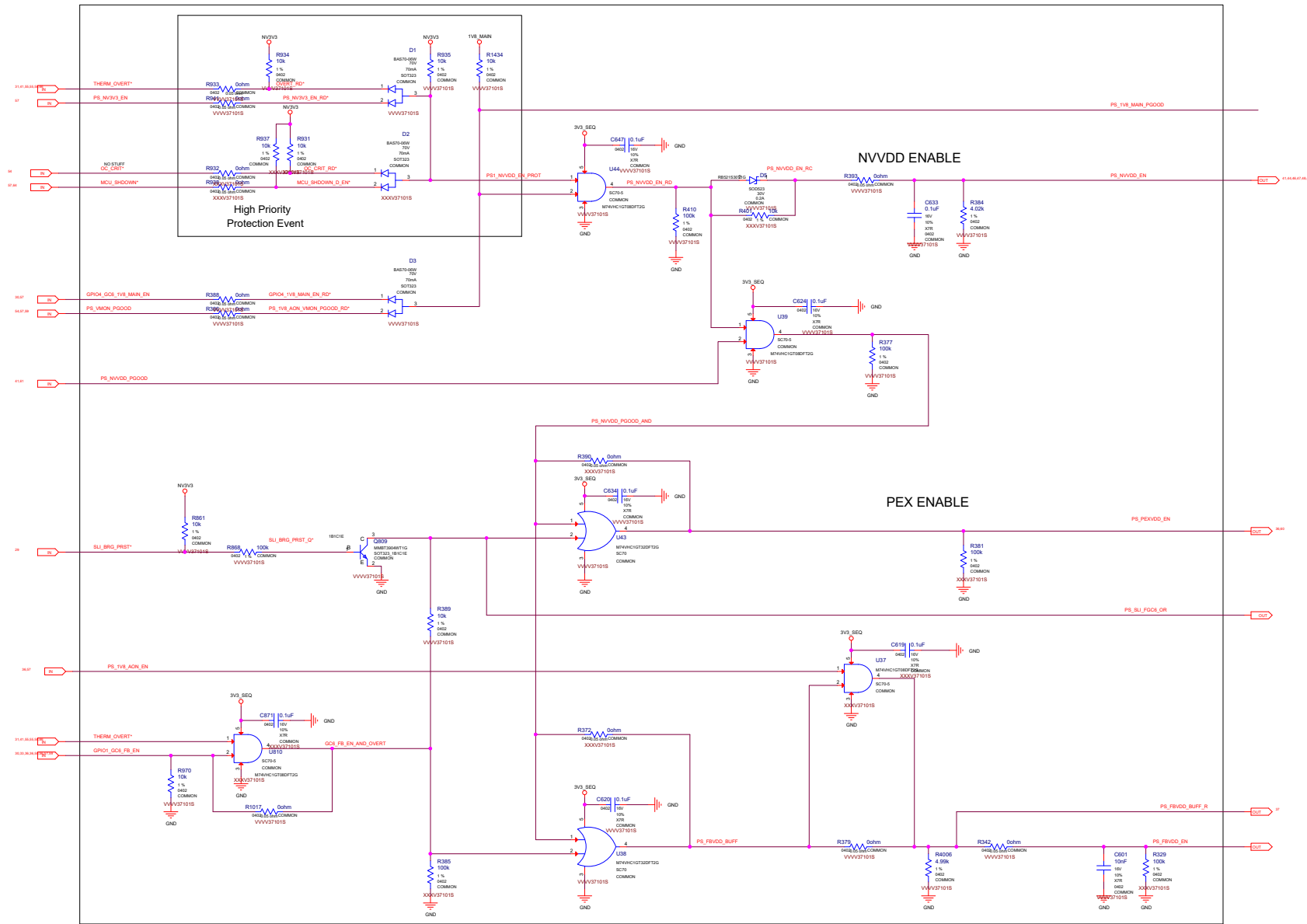
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SEQUENCE:5V,1V8,NV3V3 ENABLE



SEQUENCE:NV,PEX,FB ENABLE



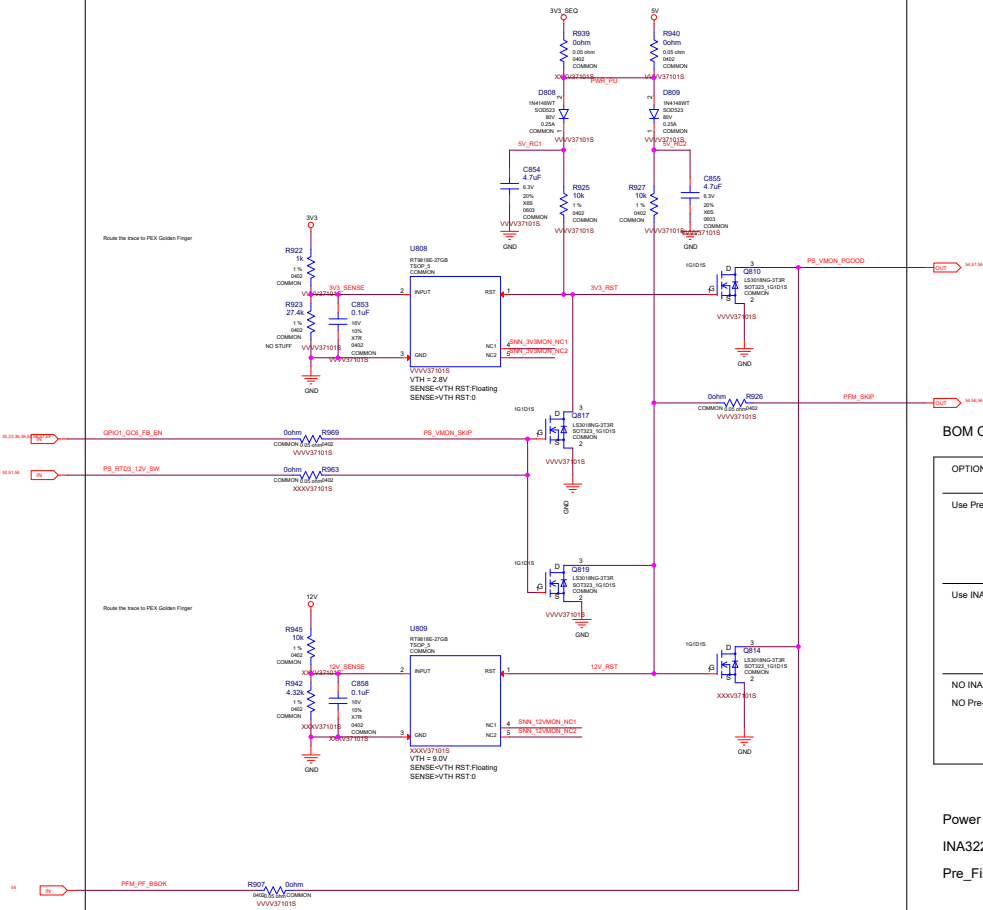
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ASSEMBLY	<ASSEMBLY_DESCRIPTION>
PAGE DETAIL	Sequence NV, PEX, FB EN

SEQUENCE:PCIE Voltage Monitor

PCIE Voltage Monitor



BOM Configuration

OPTIONS	PEX3V3_SENSE	PEX12V_SENSE	OTHER_12V_SENSE
Use Pre-Filter	Pre-Filter NO STUFF U12 NO STUFF Q3,Q5 NO STUFF D15	Pre-Filter NO STUFF U13 NO STUFF Q4	Pre-Filter
Use INA3221	Voltage_Monitor	INA3221 NO STUFF U12 NO STUFF Q4	INA3221
NO INA3221 NO Pre-Filter	Voltage_Monitor	Voltage_Monitor	N/A

Power Supply

INA3221:3V3_SEQ

Pre_Filter(ADC_MUX):3V3(PEX)

Dual Pre-Filter case:

Only use the Primary Pre-Filter to sense 3V3PEX
and All Input 12Vs

Signal	Direction	Function
3V3	INPUT	Sense the 3V3 Voltage from PCIE golden finger
12V	INPUT	Sense the 12V Voltage from PCIE golden finger
PS_VMON_PGOOD	OPEN-DRAIN	Floating(H) once both 3V3 and 12V reach Vth
GC6_FB_EN	INPUT	Indicator for RTD3/GC6 residence,Use to Mask the VMON_PGOOD
PS_PF_SKIP	INPUT	From INA3221(VPU) or Pre-filter(SKIP)
PS_PF_BSOK	INPUT	From INA3221(PV) or Pre-filter(BS_OK)
PS_RTD3_12V_SW	INPUT	GC6_FB_EN && IDLE_IN_SW

ASSEMBLY	<ASSEMBLY_DESCRIPTION>
PAGE DETAIL	Sequence PCIE Voltage Monitor

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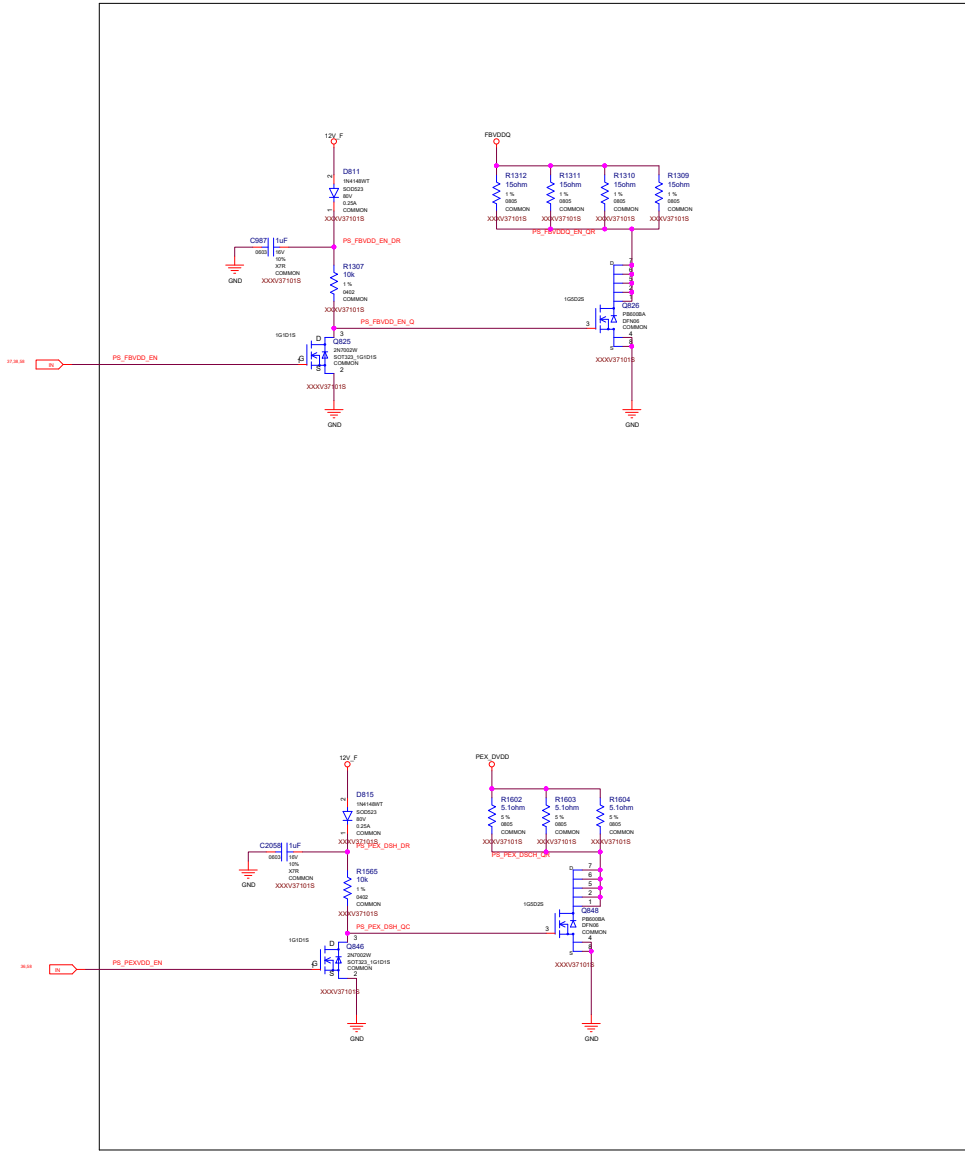
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SEQUENCE:Discharge



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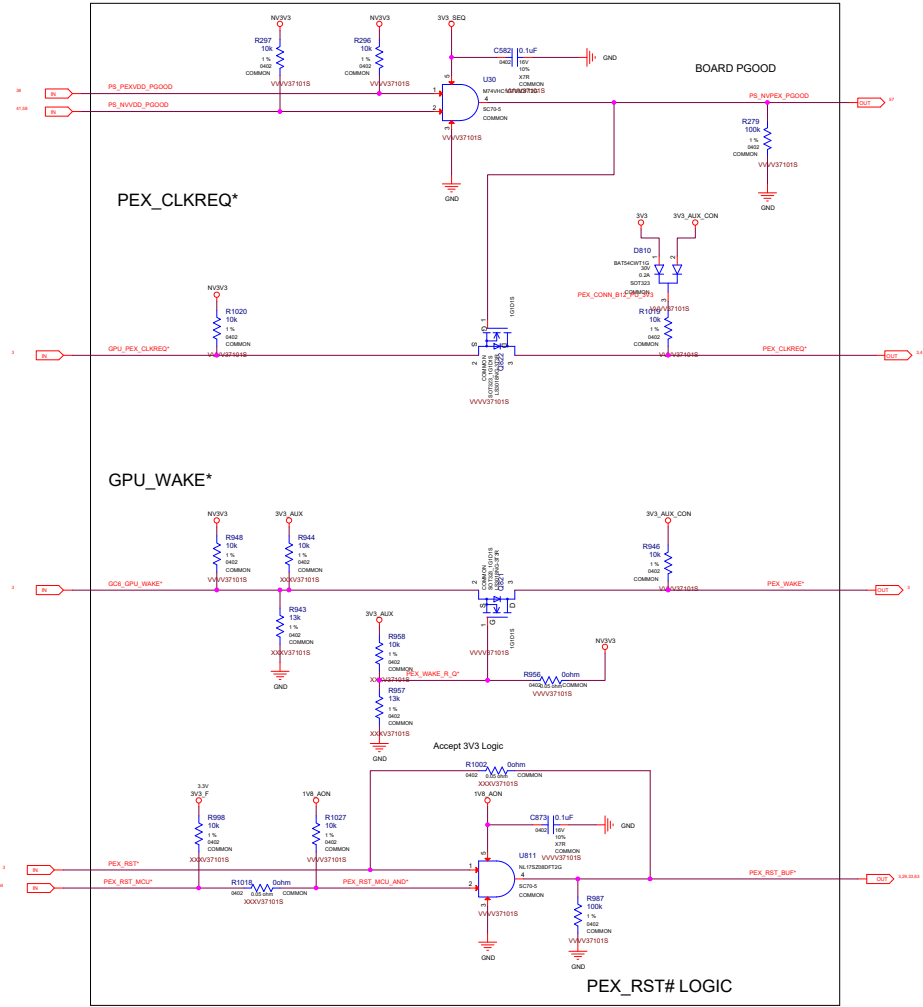


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ASSEMBLY	<ASSEMBLY_DESCRIPTION>
PAGE DETAIL	Sequence: Discharge

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SEQUENCE:MISC



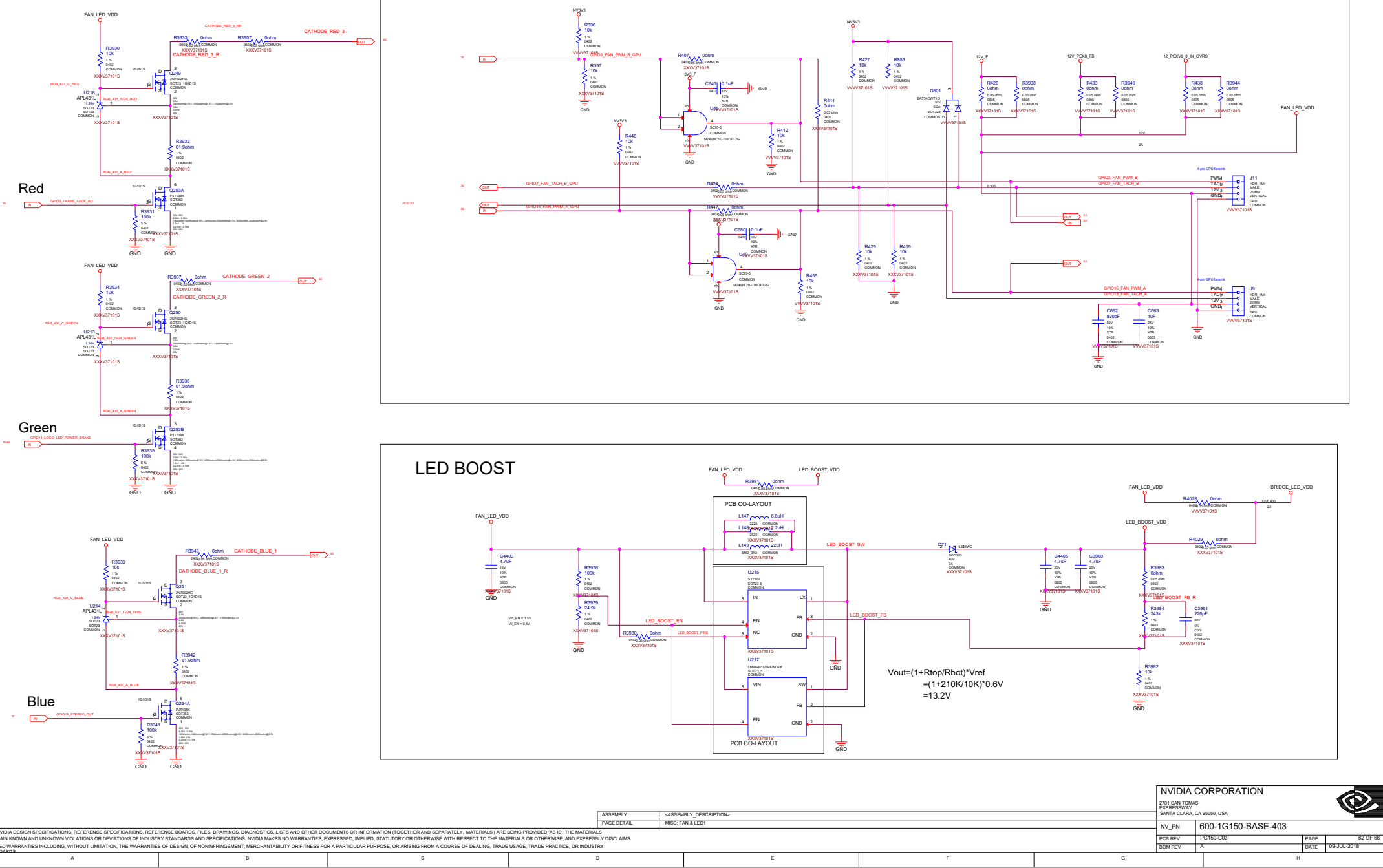
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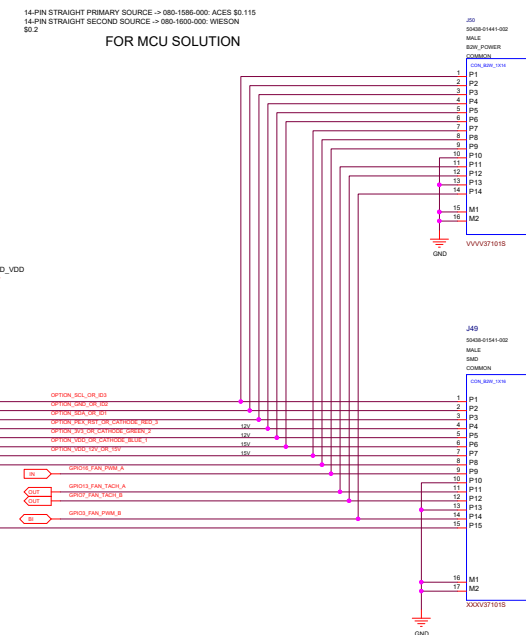
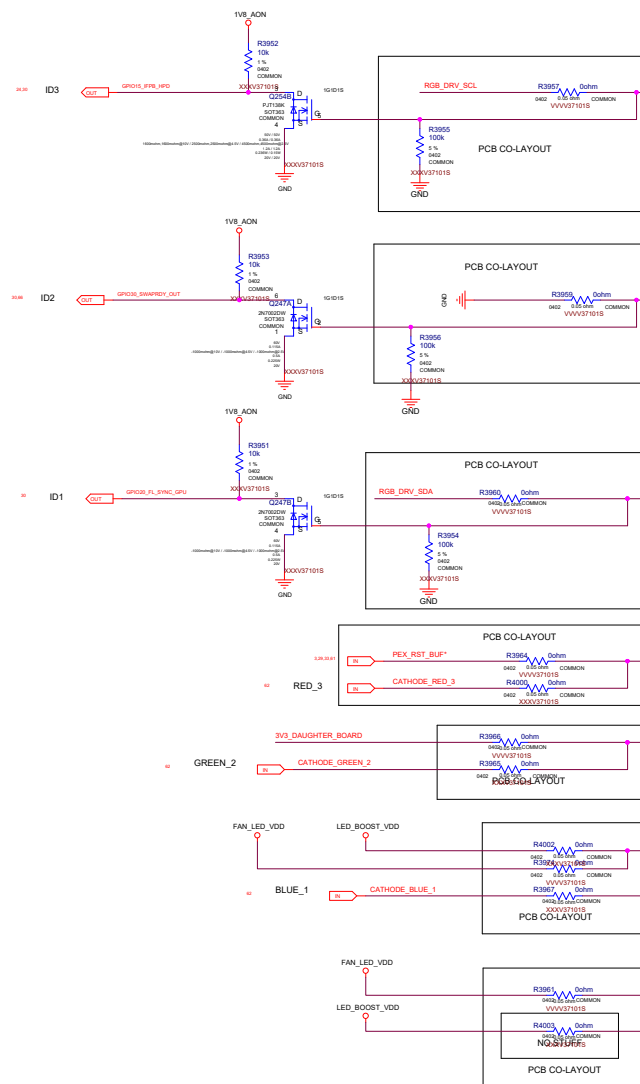
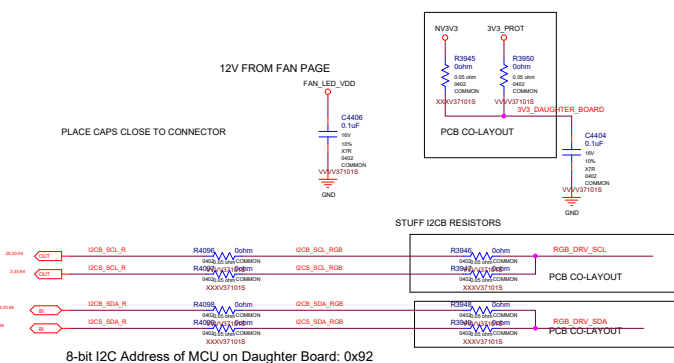
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MISC: FAN & LED1



MISC: LED2



FOR ONE ZONE RGB SOLUTION

15-PIN STRAIGHT PRIMARY SOURCE -> 080-1617-000: ACES \$0.1165
15-PIN STRAIGHT SECOND SOURCE -> 080-1628-000: WIESON
\$0.23

ASSEMBLY	<ASSEMBLY_DESCRIPTION>
PAGE DETAIL	MISCL: LED 2

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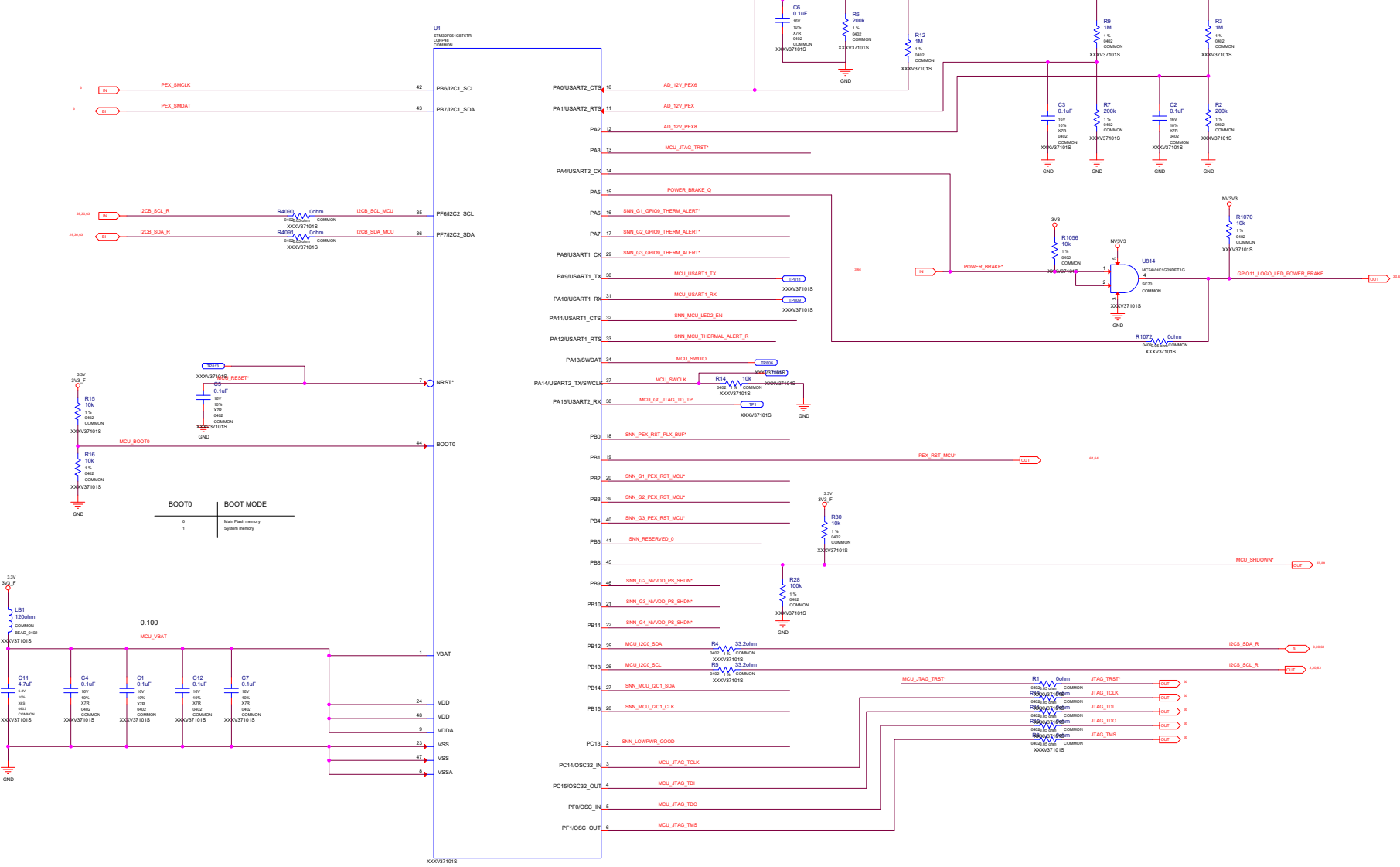
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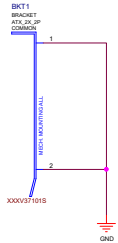
ZERO IDLE POWER MCU



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Mechanical: Bracket/Thermal Solution

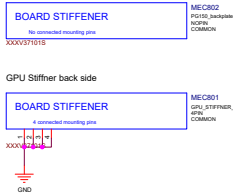
Brackets:



Bracket Screw



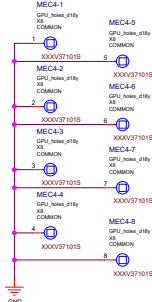
Back Cover



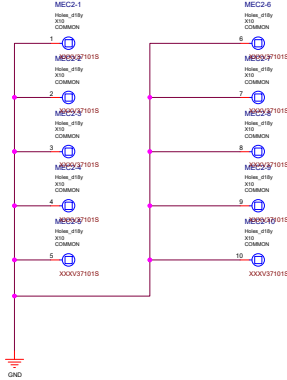
GPU Socket Symbol



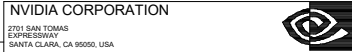
GPU Mounting holes



Mechanical Holes Symbol



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